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Yasuhiko Takemura	) Examiner: Ahmed N Sefer
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For: SEMICONDUCTOR DEVICE HAVING AT LEAST FIRST AND SECOND THIN FILM TRANSISTORS	)

Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

VERIFICATION OF TRANSLATION

Sir:

I, Asami Maruyama, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. Hei 03-296331 filed on October 16, 1991 and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. Hei 03-296331 filed on October 16, 1991.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 24th day of February 2005

Asami Maruyama

Name: Asami Maruyama

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[Title of the Invention] ELECTRO-OPTICAL DISPLAY DEVICE AND METHOD OF MANUFACTURING AND DRIVING THE SAME

[Number of Claims] 12

[Inventor]

[Address] 398, Hase, Atsugi-shi, Kanagawa-ken
c/o Semiconductor Energy Laboratory Co., Ltd

[Name] Yasuhiko TAKEMURA

[Applicant]

[Identification Number] 000153878

[Post Code] 243

[Address] 398, Hase, Atsugi-shi, Kanagawa-ken

[Name] Semiconductor Energy Laboratory Co., Ltd

[Representative] Shunpei YAMAZAKI

[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention] ELECTRO-OPTICAL DISPLAY DEVICE AND METHOD OF MANUFACTURING AND DRIVING THE SAME

[Scope of Claim]

[Claim 1] An active matrix type electro-optical display device characterized in that a signal line, a select line and a voltage supplying line are provided, and the signal line and the voltage supplying line are provided in parallel.

[Claim 2] An active matrix type electro-optical display device comprising a signal line, a select line and a voltage supplying line, characterized in that a signal applied to the select line and a signal applied to the voltage supplying line are synchronized with each other.

[Claim 3] A method of driving an active matrix type electro-optical display device, characterized in that a signal applied to a signal line is a binary value of either a signal of a positive voltage or a signal of a negative voltage in accordance with information of a pixel.

[Claim 4] An active matrix type electro-optical display device comprising a PMOS transistor and an NMOS transistor in one pixel, characterized in that a gate electrode of one of the transistors is connected to a drain region of the other transistor.

[Claim 5] An active matrix type electro-optical display device characterized in that an enhancement type transistor and a depletion type transistor are provided in one pixel.

[Claim 6] An active matrix type electro-optical display device, characterized in that an MOS transistor manufactured by a self-alignment manner and a transistor manufactured by a non-self-alignment manner are provided in one pixel.

[Claim 7] A method of driving an active matrix type electro-optical display device comprising a voltage supplying line, characterized in that an electric charge of a pixel is discharged when a signal of the voltage supplying line is in a non-voltage state.

[Claim 8] A method of driving an active matrix type electro-optical display device comprising a voltage supplying line, characterized in that a voltage of a pixel electrode is substantially equal to a voltage of the voltage supplying line.

[Claim 9] A method of driving an electro-optical display device, characterized in that digital grading is performed by using the display device according to claim 1.

[Claim 10] Regarding a manufacturing method of a pixel for an active matrix type electro-optical device, a manufacturing method of an active matrix display device characterized by comprising the steps of:

forming two MOS transistors on a substrate;

forming a contact hole for a source and a drain of a first transistor, thereby forming a signal line; and

forming a contact hole for a gate electrode of the first transistor and for a drain electrode of a second transistor, thereby forming a select line and a voltage supplying line connected to the gate electrode of the first transistor and the drain electrode of the second transistor, respectively.

[Claim 11] Regarding a manufacturing method of a pixel for an active matrix type electro-optical device, a manufacturing method of an active matrix display device characterized by comprising the steps of:

forming a select line and a gate electrode of a second transistor on a substrate;

forming an activated region of a first and the second transistors; and

forming a voltage supplying line after forming a signal line.

[Claim 12] Regarding a manufacturing method of a pixel for an active matrix type electro-optical device, a manufacturing method of an active matrix display device characterized by comprising the steps of:

forming a select line on a substrate;

forming a source region of a first transistor which is also a gate electrode of a second transistor;

forming a signal line; and

forming a voltage supplying line thereafter.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to an electro-optical display device such as a

liquid crystal display with a pixel arranged in a matrix, in particular, an active matrix type electro-optical display device. Further, the invention relates to a new pixel and a display device which can eliminate property dispersion of an active element such as a thin film transistor in each pixel or image deterioration due to an original problem of an element, and relates to a method of manufacturing and driving the same.

[0002]

[Prior Art]

Recently, a thin film transistor type liquid crystal display (TFTLCD) has been increasingly broadly utilized. TFTLCD has features that it is excellent in terms of brightness and contrast, and is easily viewable with a wide view angle rather than a conventional simple matrix type liquid crystal display, and thus, in these days, TFTLCD has been particularly actively manufactured along with the development of a color liquid crystal display.

[0003]

Fig. 2(A) shows a circuit configuration of a pixel cell of a conventional TFTLCD. In the configuration, a thin film transistor (TFT) is provided at an intersection of matrix diagonal wirings, and a gate electrode thereof is connected to a select line (also referred to as a gate line) and a drain region is connected to a signal line (also referred to as a drain line) while a source region is connected to a pixel electrode. Such a configuration itself is the same as the one which has been already employed in DRAM and reliability thereof is believed to have been fully established. However, there remain various problems practically since the operation of a liquid crystal display is partially analog while the operation of DRAM is completely digital one.

[0004]

In Fig. 2 (B), signals applied to the select line and the signal line are indicated by V_G and V_D respectively. If a liquid crystal is subjected to a direct current for a substantial time period, a characteristic of the liquid crystal is degraded by electrolysis. Therefore, a voltage signal applied to the signal line is periodically inverted (usually for each frame) in order to invert a voltage applied to the liquid crystal.

[0005]

In the diagram, a change of a voltage at the pixel electrode (V_{LC}) is also indicated when such a signal is applied. According to this, a problem of a conventional active type can be understood.

[0006]

When a voltage pulse is applied to the select line and a voltage is also applied to the signal line at the same time, the transistor is made in an ON state so that the voltage at the pixel electrode starts to increase (region t_1). This operation, however, is generally not so fast. In the case where a TFT is made of amorphous silicon, the mobility is so low that the pulse applied to the select line is sometimes stopped before the voltage reaches to the necessary level. In the case of a polysilicon TFT, such a situation is improved. However, if the operational speed is so high that the pulse width is narrower than 1 μsec, even the polysilicon TFT can no longer follow such a high speed. It takes 30 msec in the usual operation for one frame. For example, the pulse width is therefore about 50 μsec in a display in which the number of the select lines is 480 (480 rows display). If an image with higher definition or fine grading is desired, however, a frequency for the frame is necessary to be higher. Accordingly, as described above, the pulse width equal to or narrower than 1μsec is required in a high-value added product.

[0007]

The voltage at the pixel electrode then drops by ΔV as shown in the diagram at the time when the pulse to the select line is stopped. This drop, called "jump-in voltage", is caused by the parasitic capacitance which is formed by the overlap between the gate electrode and the source region. This drop is more remarkable as the parasitic capacitance increases. Thus, in the case of a pixel utilizing an amorphous TFT with a large parasitic capacitance, a capacitor is all the way provided in parallel with the pixel in order to reduce the influence of the jump-in voltage, as shown in Fig. 2(A). The provision of such a capacitor, however, increases the load on the TFT and a peripheral circuit, furthermore, the aperture ratio is decreased because of wiring work for this capacitor so that the screen becomes dark.

[0008]

In the case of a polysilicon TFT, such a problem is not so significant since a self-alignment process can be employed for manufacturing. However, ΔV about 1V still exists by the current technique, which may become a substantial problem in the future when a higher definition is required.

[0009]

The voltage at the pixel electrode gradually decreases due to discharge until a next pulse arrives after the pulse to the select line is stopped (region t_2). This discharge is mainly due to discharge from the TFT.

The pulse is then applied to the select line again. Since the voltage to the select line is inverted at this time, the voltage at the pixel electrode is also inverted and gradually changed in the same manner as in the problem described above.

[0010]

When the pulse to the select line is stopped, the minus voltage is increased this time by ΔV, and later, comes close to zero gradually due to discharge. The voltage at the pixel electrode is asymmetrical like this, thereby resulting in several problems such as flicker or deterioration of a liquid crystal.

[0011]

Furthermore, it is to be noted that such a complicated voltage change tends to vary substantially from pixel to pixel. For example, the rise of the voltage in the region t_1 depends upon the several parameters of TFT, e.g. the mobility, the channel width, the channel length, the thickness of the activated region and amounts of the gate voltage (the voltage applied to the select line) and the drain voltage (the voltage applied to the signal line). The mobility of TFT depends largely upon a manufacturing process so that the mobility is not supposed to be significantly different in the same panel. However, in the case of a large-panel liquid crystal display in the future, it is considered that the mobility depends largely upon its place. The thickness of the activated region may be also a big problem along with a development of a large panel. The dispersion in the channel width and the channel length is usually as large as about 10% by a slight difference in a mask process. In addition, the gate voltage is decreased as the select line extends, and the difference is 10% or more between the part near a driver and the

part apart from the driver. The same is also applied to the drain voltage.

[0012]

The jump-in voltage depends upon the parasitic capacitance of the TFT. In the current process, the dispersion of the capacitance is about 20% in the case of a non-self alignment process and about 10% in the case of a self-alignment process. Furthermore, the jump-in voltage is in proportion to the gate voltage so that the dispersion of the parasitic capacitance and the dispersion of the gate voltage form a multiplier action to the jump-in voltage since the gate voltage varies depending on a place in the panel as described above.

[0013]

On the other hand, the decrease of the voltage at the pixel due to discharge depends largely upon the channel length, the channel width and a characteristic of the activated region of the TFT. As a result, the voltage at the pixel varies from the one indicated by a solid line to the one indicated by a broken line.

Particularly accurate quality control is required for manufacturing a device in order that such dispersion of the voltage is within an aimed range. As a result, product yield is significantly decreased. It is profitable with this yield in a current low-value added product with low quality; however, it may be impossible to profit with a current product level in order to manufacture a highly-value-added product which may be required in the future.

[0014]

At the present time, a grading display in TFTLCD can be performed by controlling the voltage to the signal line at appropriate level. However, the grading display seems to be impossible even with 16 grades from the view point of reality. The threshold voltage of a usual TN liquid crystal is around 5V, which is divided by 16 into 300mV. Considering the voltage rise and its dispersion, the amount of the jump-in voltage and its dispersion and dispersion in discharge, the variation is about 300mV unless products are carefully sifted out.

[0015]

From the above view point, the present inventor and other have advocated a

digital grading display system in place of a conventional analog grading display. The digital grading display is realized by controlling the time for which a liquid crystal is subjected to a voltage, and is described in Japanese Patent Application Nos.Hei3-169305, Hei3-169306, Hei3-169307, Hei3-209869 and the like, for example. However, an operation speed is required to be 20 to 300 times as fast as a conventional driving speed, and a CMOS TFT has to be developed because it is difficult to drive with an NMOS TFT alone. In the present situation, it is also difficult even with such a technique to suppress disturbance of grading due to property dispersion of each TFT.

[0016]

For example, when it is intended to perform an intermediate display by making 45% of one frame a voltage state, 110% of the aimed voltage may be applied to a certain pixel whereas 90% of the voltage may be applied to the other pixel. In that case, the difference in brightness is 20% or more such as 1.1 x 45% = 49.5% in the former and 0.9 x 45% = 40.5% in the latter. Thus, in the actual situation, only 8 grades seem to be possible.

[0017]

In order to solve this problem, as described in Japanese Patent Application No.Hei3-209870, for example, which is an invention by the present inventor and other, a method is proposed in which a characteristic of each pixel is inputted into an external memory device in advance, and an image signal is processed by this data and sent to the pixel. The data processing, however, is so complicated that a peripheral driving circuit must carry heavy burden. Furthermore, it takes a substantial time to examine the respective pixels and input correction data (if the examination and input for one pixel takes one second, 85 hours are necessary in the case of a panel of 640 x 480), resulting in a increased cost.

[0018]

[Problems to be solved by the Invention]

The present invention is made in order to cover a disadvantage of the conventional TFTLCD as above or LCD of a digital grading system which is developed by improving the TFTLCD. First, in the invention, a structure is suggested, in which a

characteristic of an LCD panel is not affected directly by each TFT. When a characteristic of each TFT is not directly reflected to an image quality, a tolerance range of dispersion in TFTs is wider, thereby increasing yield and reducing a product cost. The invention advocates a structure particularly suitable for a driving method of a digital grading system, and notes the driving method. In addition, the invention suggests a structure suitable for obtaining a high added-value by a fast operation including the digital grading system. Furthermore, a process suitable for manufacturing the structure as above is also noted.

[0019]

[Means for solving the Problems]

According to the idea of the present invention, when a pixel electrode is in a voltage state, a stable voltage should be always supplied. Accordingly, a voltage, which is decreased due to discharge with time as conventionally, is prevented from applying. For this purpose, a driving circuit as shown in Fig. 1 (A) is employed.

[0020]

This circuit includes two transistors, and a gate (G_1) of a first transistor Tr_1 is connected to a select line V_G and a drain (D_1) is connected to a signal line V_D. This condition is the same as in a conventional TFTLCD; however, a source of Tr_1 is connected to a gate electrode of a second transistor Tr_2 in the invention. Furthermore, a drain of Tr_2 is connected to a voltage supplying line V_{LC}, and a source of Tr_2 is connected to a pixel electrode. As above, the invention is characterized by applying a mechanism to transmit a signal of the signal line indirectly to the pixel electrode. In the case where the signal of the signal line is directly connected to the pixel as conventionally, there are many limits in operation time; however, there is enough time by connecting indirectly to the pixel.

[0021]

More specifically, the signal of the signal line itself is not applied to the pixel electrode, thus, even if the signal passed through Tr_1 deviates significantly from a predetermined level, the pixel electrode is always supplied with a constant voltage as long as the deviating level is in a range to be controlled by Tr_2.

[0022]

Namely, as discussed above, the width of the signal pulse of the select line is extremely short, e.g. 70 μsec for a typical case, and in a special case for performing digital grading, the width is from a tenth or more to a several-hundredth of that in the typical case. For such a short time, the voltage accumulated at the pixel electrode eventually tends to vary significantly because of property dispersion of each TFT.

[0023]

On the other hand, when the operation of the invention is analyzed, the width of the voltage pulse applied to Tr_1 is also very short, and its source voltage varies largely. However, since the voltage is not applied to the pixel electrode but applied to the gate electrode of Tr_2 that is the second TFT, it is enough as long as the source voltage of a TFT with the lowest property can sufficiently control Tr_2, even if there is dispersion depending on each TFT to some extent.

[0024]

If such a condition is satisfied, a constant voltage can be supplied to the pixel electrode from the voltage supplying line V_{LC} by controlling ON/OFF of Tr_2. Accordingly, an amount of the voltage applied to the pixel electrode is not dictated by the signal from the signal line. The signal from the signal line only transmits ON or OFF.

[0025]

Furthermore, it should be noted that the operation of Tr_2 itself can be significantly slower than that of Tr_1. It is possible that Tr_2 operates after completion of the ON/OFF operation of Tr_1 since an electric charge is trapped at the gate electrode of Tr_2 by Tr_1, and thus, Tr_2 can react during a sufficiently long time until a next signal is sent to Tr_1 again. As a result, Tr_2 can be formed of an amorphous silicon TFT having a slow operation speed even for performing digital grading with about 32 grades, for example.

[0026]

Furthermore, in a configuration of Fig. 1 (A), the load upon Tr_1 is significantly reduced as compared with that in a conventional TFT. In the conventional

configuration, all the electric charges sent to the pixel electrode must pass through the all TFTs within a short time which is 70 μsec at a maximum. However, in the invention, an electric charge passing through Tr_1 corresponds to the capacitance formed between the gate and the drain of Tr_2. For example, in the case where the area of the pixel is 300 μm x 300 μm and the thickness thereof is 6 μm, and where the area of the gate electrode of Tr_2 is 10 μm x 10 μm and the thickness of the gate insulating film is 0.2 μm, the capacitance of the former is 30 times as large as that of the latter. In addition, when the area of the gate electrode is made further smaller, 5μm x 5μm for example, the capacitance becomes 120 times larger.

[0027]

It is apparently understood that a TFT carries a heavy load in a conventional technique. On the other hand, in accordance with the invention, the load on Tr_1 can be a 30th to a 120th of that in the conventional TFT, or less than that. This means that the speed of Tr_1 can be 30 to 120 times as fast as that in a conventional system, or faster than that. For example, as long as the conventional system is employed, digital grading can not be realized with an amorphous silicon TFT since the mobility of amorphous silicon is very low and a fast operation with a large movement of an electric charge as conventionally is impossible.

[0028]

The amount of the electric charge, however, is significantly small in accordance with the invention as compared with the conventional case so that the above problem is not the major one. Accordingly, it is possible to drive an amorphous silicon TFT with a speed about 100 times as fast as the conventional case in order to realize digital grading of 64 or more grades.

An amorphous silicon TFT can be produced at a relatively low temperature as compared with a polysilicon TFT so that mass production is facilitated and the production cost is reduced.

[0029]

On the other hand, as for an operation of Tr_2, Tr_2 operates sufficiently with a speed of a 100th of that in Tr_1 or faster, preferably a 20th or faster. In this case, the

amount of an electric charge passing through Tr_2 is equal to that in the conventional case. However, since the speed can be slow, an amorphous silicon TFT can be employed as Tr_2 for digital grading with 32 grades, for example. In that case, when the switching speed of Tr_2 is 70 μsec, similarly to the conventional amorphous silicon TFT, Tr_2 operates with no problem since the operation speed thereof is only 7% of the minimum cycle of the digital grading, i.e. a 32nd of 33 msec, which is about 1msec. Of course, the polysilicon TFT can ensure a sufficient capacitance.

[0030]

The channel width of Tr_2 can be increased for the purpose of increasing the operation capability of Tr_2 in order to realize more fine grading display. Care must be paid in this case because the capacitance between the gate and the drain of Tr_2, which is the load on Tr_1, is increased. For example, if the channel width is five times larger, the driving capability of Tr_2 is five times increased; however, the load on Tr_1 is also five times increased so that the operation speed of Tr_1 is reduced to 20%.

[0031]

Referring to Fig. 1(B), an example of a driving method in Fig. 1(A) will be described. The select line and the signal line are supplied with a signal as conventionally. Note that a signal inputted to the signal line is a pure digital signal. On the other hand, the voltage supplying line is supplied with a signal which becomes positive or negative alternately. This signal repeats in the same cycle as in the select line. The signal to the voltage supplying line is set at 0 during the time for which the select line is supplied with a pulse in this example. Signals of the select line, the signal line and the voltage supplying line are indicated by V_G, V_D and V_{LC} respectively in the diagram.

[0032]

The voltage change at each point in the circuit is checked. The voltage at V_1 and V_2 in Fig. 1 (A) are indicated by V_1 and V_2 in Fig. 1(B). First, the voltage V_1 at the source side of Tr_1 rises as indicated by a solid line due to signals from the select line and the signal line, and then lightly drops by a jump-in voltage responsive to a stop of a pulse of the select line. After that, V_1 gradually decreases due to discharge.

[0033]

On the other hand, the voltage at the source side of Tr_2, i.e. the voltage at the pixel electrode changes as follows: Tr_2 is made in an ON state since V_1 is in a voltage state. Next, since a voltage is supplied to the voltage supplying line, the pixel electrode is charged by this voltage. In this situation, it is noted that since Tr_2 is already in an ON state, the charging is substantially dictated by the ON resistance of Tr_2 and the capacitance of the pixel electrode, resulting in a significantly rapid onset.

[0034]

In the invention, a signal is normally sent to the voltage supplying line only when a certain time elapses after the pulse of the select line is stopped. Of course, it is also possible to supply the voltage to the voltage supplying line just after the pulse is stopped. However, this is not suitable way, when a fine grading display is performed by means of a TFT having a particularly slow operation speed as Tr_2 in accordance with the digital technique (particularly such a technique as described in Japanese Patent Application Nos.Hei3-163870, 3-163871, 3-163872, 3-163873 which are inventions by the present inventor or other).

[0035]

For example, consider a digital grading display with 64 grades. The minimum periodic cycle of the pulse of the select line is 500 μsec. Although the width of the select pulse is 1 μsec in the case of a matrix having 480 rows, Tr_1 can operate sufficiently because of the light load thereon as explained above. There arises no problem, even if the voltage at the source side of Tr_1 rises not so much, as long as the sufficient voltage to drive Tr_2 is supplied. Accordingly, there is no problem to Tr_1. That is, the source side of Tr_1 is in a sufficiently high-voltage state, when the pulse of the select line is stopped (after 1 μsec of sending the pulse of the select line).

[0036]

Tr_2 is designed to have the lowest driving capability and requires 70 μsec to be in an ON state here. However, there may be a TFT with excellent property in a panel, and a TFT corresponding to Tr_2 in a certain pixel can be in an ON state by 60 μsec. Such disparity originates from a combination of a difference in mobility due to a slight

difference in the film quality of an activated layer and a difference in the channel width and channel length due to slight variation of a photomask.

[0037]

If the voltage is supplied to the voltage supplying line V_{LC} just after the select pulse is stopped or during the time for which the select pulse continues in a panel in which TFTs with various properties are provided, charging is completed after 60 μsec in one pixel, but it takes 70 μsec in the other pixel to complete charging. That difference of 10 μsec, which seems sufficiently small, is equal to 2% of the minimum periodic cycle of 50 μsec.

[0038]

Actually, such large dispersion of 2% makes 64 grades-display meaningless because the dispersion of duration time of the pulse for each pixel must be limited within 1.6% in order to realize 64 grades. Of course, the dispersion can be suppressed by aligning a TFT property. The yield, however, is significantly reduced as a result, which is not intended by the invention.

[0039]

On the other hand, if the voltage is supplied to the voltage supplying line when 80 μsec or 100 μsec elapses after the pulse of the select line is stopped, all the Tr_2s are in an ON state and all the pixels are in a voltage state at the same time point. In this case, the time needed until charging is influenced by parameters of a pixel such as the pixel capacitance and the ON resistance of Tr_2. The ON resistance is around 10^6 Ω and the pixel capacitance is around 10^{-13} F so that the time constant is about 100 nsec at this time.

[0040]

Accordingly, even if the time constant is dispersed from pixel to pixel, unless the dispersion does not exceed 50% of the time constant, it is the dispersion of 100 nsec which is extremely small as compared with the periodic cycle of 500 μsec (0.02%) and meets a requirement of the above described 64 grades (dispersion is within 1.6%).

As a result, it is effective for a finely grading display to supply the voltage to the voltage supplying line after a certain time.

[0041]

Similar attention has to be paid when the voltage is removed from the voltage supplying line. In this step, it is desirable to remove the voltage from the voltage supplying line before the pulse is applied to the select line in order to certainly discharge an electric charge accumulated in the pixel.

[0042]

For example, if the voltage supplying line is in a voltage state even when the select pulse is applied, an electric charge accumulated at the gate electrode of Tr_2 disappears in the case where Tr_1 is not selected (namely, a signal is not supplied to the signal line). Then, Tr_2 is made in an OFF state automatically, and the electric charge remains in the pixel despite the intention as a result.

[0043]

In order to avoid such a case, all the electric charges accumulated in the pixel are desirably discharged, setting the voltage of the voltage supplying line at 0, before the pulse is supplied to the select line. The certain time period τ is needed until the voltage of the voltage supplying line is set at 0 and the select pulse is applied. However, the time required for discharge of the electric charges is around the above time constant, and thus particular attention is not needed.

[0044]

In the second cycle, the voltage of the voltage supplying line is negative and is made to be alternating. The negative voltage is supplied to the voltage supplying line also after the select pulse is stopped and the certain time period elapses.

The polarity of the signal of the signal line is inverted to be alternating in the conventional case; however, in the invention, the polarity of the signal of the signal line dose not need to be inverted as shown in Fig. 1(B).

[0045]

As is apparent from the diagram, voltage change due to the jump-in voltage as conventionally is observed only in V_i, and is not observed in the voltage applied to the pixel. Decrease due to natural discharge is not observed, either. This is because the

voltage applied to the pixel is electrostatic accumulated at the pixel electrode in the conventional case, whereas the voltage applied to the pixel is always supplied from the constant voltage supplying line in the invention. The invention has a feature in this difference.

[0046]

Furthermore, for the purpose of considering dispersion of an element, a broken line is plotted in the diagram to show the case where a characteristic of Tr_1 is poor. Namely, because of the poor characteristic of the element, the rise of the source voltage of Tr_1 is insufficient so that the source voltage can not reach to the drain voltage, and the parasitic capacitance is large so that the influence by the jump-in voltage is remarkable, in addition, natural discharge is large. In the case where such a TFT and a TFT having a characteristic indicated by a solid line are provided in the same panel, the panel in accordance with a conventional technique has a problem of irregular colors and cannot be used, whereas there are no problems in the invention.

[0047]

That is, even if a TFT exhibits such a characteristic as shown by a broken line, there is no influence on the pixel electrode as long as the final source voltage (when the voltage of the voltage supplying line becomes 0) is enough to control Tr_2.

[0048]

As shown in the diagram, even if V_1 is indicated by a broken line, no influence appears on V_2. Conventionally, it was the most important issue to reduce dispersion of this voltage V_1 as less as possible. Therefore, yield was not increased, thereby resulting in the high production cost. In accordance with the invention, even a panel, which was thought to be defective conventionally, can be used with no problem.

[0049]

For example, in the case of a panel including not a few TFTs which have a characteristic as indicated by a broken line at V_1 in Fig. 1(B), the voltage of the select line and the signal line may be set so high that the voltage is equal to or more than the threshold voltage of Tr_2, for example. Of course, the voltage must not be set too high so that a non-defective TFT is not destroyed.

[0050]

Practically, in accordance with an experiment conducted by the present inventor or other using a small scale panel of 10 rows x 10 columns (100 elements), it was very easy to form 90% or more TFTs having V_1 capable of providing 5V or higher in the case where the select pulse is 15V high and the voltage of the signal line is 10V. In this step, the yield was 95% or more. In this case, when the gate voltage and the drain voltage of the TFT are furthermore increased by 5V, 5V or higher is achieved in 99% of the TFTs without a destructed TFT by such an operation.

[0051]

However, if a conventional technique is applied, even a black-white display is difficult in such a panel. Namely, in the above panel, V_1 is 7.2V in average and only 60% thereof is within a range of ±0.9V. This means that 40% of the TFTs were inappropriate even for realizing a grading display with only 8 grades. When panels are selected in order that 90% or more TFTs are within a range of $V_1 = (7.2 \pm 0.9)$ V, the yield is significantly decreased. Of course, this experiment was not conducted under the best condition so that it may be possible to improve the yield by optimizing the condition. The production of a larger scale display, however, requires a large amount of work.

[0052]

In accordance with the invention, at least two TFTs have to be provided for one pixel and it is concerned that the yield can be therefore reduced. The requirement upon the characteristic of the TFT, however, is significantly low compared with the one by a conventional technique as described above so that the yield is not reduced by this configuration itself.

[0053]

In the case of Fig. 1, the select line and the voltage supplying line are provided for each row, and therefore, a wiring is twice increased than in the conventional technique, resulting in a problem of decreasing the aperture ratio of the pixel. Actually, in a conventional liquid crystal display device, particularly the one utilizing an amorphous silicon TFT in which the parasitic capacitance at a TFT is a problem, it is

needed that a wiring is formed in parallel to a select line and used as a supplemental capacitance wiring. Therefore, it is not so disadvantageous that the wiring density is increased to lower the aperture ratio as compared with the conventional technique. However, in the case of considering a terminal connection, a double mounting density is required. This problem can be solved by employing a configuration shown in Fig. 3.

[0054]

Fig. 3(A) shows a configuration in which a pair of adjacent pixel rows is formed to share a voltage supplying line. By employing such a configuration, the wiring density is reduced by 25% as compared with the configuration of Fig. 1 and the mounting density is suppressed to half as high again as that of a conventional ideal active matrix type. In the same manner, one voltage supplying line can be provided for three adjacent pixel rows, or more than three rows can share one voltage supplying line. All pixel rows can share a voltage supplying line, however, a pixel needs to have a special configuration and further it is required to drive specifically in that case.

[0055]

A driving example of Fig. 3(A) is explained using Fig. 3(B). V_G and V_G' indicate a signal of the upper and lower select lines respectively, V_D indicates a signal of the signal line and V_{LC} indicates a signal of the voltage supplying line. Further, a solid line in V_1 and V_2 indicates a voltage in V_1 and V_2 (upper pixel), and a broken line indicates a voltage in V_1' and V_2' (lower pixel) in Fig. 3(A). A signal of the select line and a signal of the signal line are the same as in the conventional case or the case of Fig. 1. However, the signal of the voltage supplying line is different from the case in Fig. 1 and it is not in a voltage state when the pulse of both upper and lower signal lines is continued. Namely, it is necessary that an electric charge of both upper and lower pixels moves.

[0056]

First, the pulse is given to the upper select line. TFT (Tr_1) at the upper pixel is made in an ON state and V_1 is in a voltage state because a signal has already come to the signal line. Therefore, the second TFT (Tr_2) at the upper pixel is also made in an ON state. Then, the pulse is given to the lower select line, however, V_1' is not made in

a voltage state since the signal line is no longer in a voltage state at that time. Thus, TFT (Tr_1') at the lower pixel is maintained in an OFF state and the second TFT (Tr_2') at the lower pixel is also maintained in an OFF state.

[0057]

On the other hand, after the pulse of both select lines is stopped, a signal is sent to the voltage supplying line which is used in common. As a result, the voltage is supplied to the upper pixel electrode through Tr_2 which is in an ON state and the pixel is in a constant voltage state. However, in the lower pixel, the pixel electrode is not in a voltage state since Tr'_2 is in an OFF state.

[0058]

Thus, one cycle is completed and the pulse is sent to the select line of this pixel again. Right before or at the same time of this process, the pulse of the voltage supplying line is stopped and an electric charge in the upper pixel which was in a voltage state flows through Tr_2 which is in an ON state, thus, the upper pixel is not in a voltage state.

[0059]

This time, the upper pixel is not selected by the pulse of the select line and the signal of the signal line, but the lower pixel is selected. Therefore, Tr_1 is maintained in an OFF state and Tr_2 is also maintained in an OFF state, whereas Tr_1' is in an ON state and Tr_2' is maintained in an ON state.

After that, the voltage is added to the voltage supplying line and is added to the lower pixel electrode through Tr_2' which is in an ON state. The voltage is not applied to the upper pixel electrode.

[0060]

In Fig. 3, it is shown that a transistor property of the two TFTs, namely Tr_1 and Tr_2, are significantly different from each other by comparing the voltage at V_1 and V_1'. Tr_1 has an excellent property such as a quick voltage rise, small decrease of the jump-in voltage and small natural discharge. On the other hand, all those properties are deteriorated in Tr_1'. Usually, if such TFTs having significantly different properties are formed on the same display, dispersion is large and the display cannot be used as a

display requiring a fine operation such as a grading display.

[0061]

However, in the invention, even if the property of Tr_1' is deteriorated than the other TFTs, the constant voltage is supplied to the pixel electrode and dispersion or the like is not caused as long as the voltage is equal to or more than the threshold voltage of the second TFT, namely Tr_2', or desirably equal to or more than the voltage applied to the voltage supplying line in one cycle. That is, a panel (TFT), which was conventionally thought to be defective, can be used. For this purpose, the voltage of the signal line and the voltage of the select line may be adjusted so that a TFT having the lowest property fulfill the above condition. A panel, which has been supposed to be defective, can be used as a result, therefore, yield can be increased and the manufacturing cost can be reduced.

[0062]

It will be described with reference to Fig. 4 that a TFT having a low property can be sufficiently used according to the invention, whereas it has been conventionally considered that such a TFT can be hardly used.

Fig. 4(A) shows a circuit used in the invention. It is known that a parasitic capacitance of a TFT exists therein in addition to a necessary TFT and a pixel (also functions as a capacitor and denoted by C_3), and such a parasitic capacitance causes a problem in a liquid crystal display.

[0063]

The typical problem is the jump-in voltage which has been already explained many times. Due to a parasitic capacitance C_1 between the gate and the source of the TFT, the capacitor at the source side (capacitance of the pixel electrode in the conventional circuit, the capacitance between the gate and the drain of the second TFT, Tr_2, in the invention) and the gate wiring are coupled capacitively, therefore, the voltage is changed. The voltage width ΔV in Fig. 4 is calculated by the following equation.

$\Delta V = C_1 V_G / (C_1 + C_2)$

In the invention, the amount of C_2 is dictated by the area of the gate electrode and the thickness and the dielectric constant of the gate insulating film of Tr_2. In particular, in

accordance with the invention, it is advantageous to make this capacitance small in order to reduce the driving load on the first TFT, namely Tr_1. For example, the capacitance of the pixel can be 1% or less. With such a small load, the operation, 100 times as fast as the conventional display, can be realized.

[0064]

In this case, however, the parasitic capacitance of Tr_1 can not be neglected sometimes. Typically, the amount of C_1 may be equal to that of C_2. In a conventional TFT, C_1 is always smaller than the pixel capacitance by one order of magnitude in any case. Thus, the voltage change is a problem but a percentage thereof has not been so large. If C_1 equals C_2, a half of the voltage applied to the gate electrode is changed. Fig. 4(B) illustrates an example thereof.

[0065]

In Fig. 4 (B), the voltage V_G (solid line) applied to the gate electrode of Tr_1, namely N channel type TFT, and the voltage V_D (broken line) applied to the signal line (drain wiring) are shown in the upper part. In the lower part, the voltage change at the source side is shown. V_G is assumed to be 30V and V_D is assumed to be 20V, for example. When the voltage is applied to the gate electrode, the voltage rises to 20V and becomes constant. However, at the time when the gate voltage becomes 0, a half of the voltage V_G is lost due to the influence of the jump-in voltage and V_G drops. Namely, the voltage drops by 5V and only 5V remains consequently.

[0066]

Such a situation is not fatal to the invention. As long as the voltage around 5V remains even if a TFT having the lowest property is used, this is equal to or more than the threshold voltage of Tr_2 and the pixel can be supplied with the voltage. Of course, in the case of other TFTs having a better property, the voltage drops not so largely and the voltage of 10V or more is applied to the gate electrode of Tr_2. However, the voltage applied to the voltage supplying line is supplied to the pixel in any TFT evenly, and thus there is no problem of irregular colors or the like. In the conventional technique, dispersion of a TFT property causes deterioration of an image quality. If the voltage is increased to cope with the TFT having the worst property, too high

voltage is applied to a liquid crystal in a pixel having a TFT of the best property. In the invention, there is no concern about this. It is because, when the worst TFT is a basing point, the highest voltage is applied to the gate electrode of Tr_2 which has a withstanding voltage from several times to ten and several times as high as that of a liquid crystal material.

[0067]

A view point was introduced that such a voltage drop is not a particular problem in the invention; however, this could be a serious problem from other aspects. Namely, since the pulse with quite high voltage passes around, its power consumption can be increased. If the high voltage such as 30V leaks, other driving circuit and equipment can be damaged seriously, furthermore, a human body can be also damaged. This problem can be solved by a method as shown in Fig. 4(C).

[0068]

In Fig. 4(C), the positive voltage is applied to the gate electrode and the negative voltage is applied to the drain electrode. Namely, the electric potential difference between the gate electrode and the drain electrode is 10V, and the same driving capability of the TFT as in the case of Fig. 4(B) is expected. For example, V_G is set at 5V and V_D is set at -5V.

[0069]

Next, the voltage change at the source side is observed. When the voltage is applied to the gate electrode, the voltage is increased negatively at first and equals the drain voltage. When the voltage at the gate electrode becomes 0, the negative voltage sometimes increases on the contrary due to the influence of the parasitic capacitance of the source voltage. The negative voltage is 2.5V, which is half of the gate voltage, and the voltage at the source side becomes -7.5V at last. For example, if Tr_2 may be a P-channel type transistor or a depletion type transistor which is driven by the negative voltage, voltage of both the select line and the signal line can be a single voltage of 5V, thereby realizing significantly low power consumption and solving a problem of safety.

[0070]

It is noted that the voltage of -2.5V is applied to the source side due to the

change of the gate voltage in this case even if the voltage of the signal line is 0. In a normal amorphous silicon TFT, not so many troubles are caused at around this voltage, however, it results in an ON state when the threshold voltage of Tr_2 is small by a polysilicon TFT. Therefore, a signal state can be also generated even if it is intended that there is no signal. Such a trouble can be avoided by supplying a negative voltage in the signal state and a positive voltage in the non-signal state to the drain of Tr_1. In that case, the signal state is like the one shown in Fig. 4 (C). In the non-signal state, the voltage at the source side is +2.5V and there is no response when Tr_2 is P-channel type or depletion type.

[0071]

In the invention, an electric charge accumulated in the capacitor of the pixel cannot be directly eliminated by the pulse of the select line, which is a different point from the conventional technique. Accordingly, as explained above, an electric charge is eliminated by making the voltage of the voltage supplying line 0 when Tr_2 is in an ON state. This is enough but the third TFT, Tr_3, which is connected to the pixel electrode and can be controlled by the select line, may be provided as shown in Fig. 5(A) in order to discharge more effectively. In this case, Tr_3 discharges an electric charge accumulated in the pixel electrode during application of the pulse to the select line. However, the jump-in voltage due to the parasitic capacitance of Tr_3 causes an unexpected voltage change of the pixel electrode. There is no problem, however, concerning the voltage change as long as the parasitic capacitance is substantially smaller than the capacitance of the pixel electrode.

[0072]

Alternatively, a configuration may be provided in which a resistance may be inserted in parallel to the pixel as illustrated in Fig. 5(B) in order to promote natural discharge. The value of the resistance R may be set so that the time constant with the pixel is about one frame, e.g. 33 msec when used in usual type. If digital grading is performed and faster discharge is desired, it is selected to be 500 μsec for 64 grades or about 125 μsec for 256 grades in order to discharge so that clear images without afterimages and blurs can be obtained.

[0073]

When a display is provided with the pixel electrode accumulated with an electric charge as conventionally, it is difficult to provide a circuit in which a voltage (electric charge) decreases for such a short time because of instability of the pixel voltage. Even if such a resistance is provided, it is inevitable that dispersion of resistance value is around 20%. Therefore, the voltage decreases during one frame at a different rate and dispersion in the voltage is about 20% after one frame is completed.

[0074]

In accordance with the invention, however, the voltage at the pixel electrode equals the voltage of the voltage supplying line and it is constant most of the time. Thus, display dispersion due to the difference of the resistance value is not a big problem.

[0075]

In Fig. 5(B), the resistance is provided in parallel to the pixel electrode. Such a configuration requires further additional wiring to be formed, and it should be noted that the aperture ratio can be lowered.

[0076]

In the invention, an efficient operation is realized by a combination of NMOS and PMOS (CMOS) or a combination of an enhancement type and a depletion type as described in the explanation in Fig. 4.

[0077]

Fig. 6 illustrates a combination of an enhancement type and a depletion type. Namely, an enhancement type TFT is used as Tr_1 and a depletion type TFT is used as Tr_2. The operation at this time is shown in the following diagram.

[0078]

Here, in the voltage indication of the signal line V_D, a positive signal is to be ON and a negative signal is to be OFF. At first, when the pulse of the select line is applied, the voltage of the signal line is to be positive in order to transmit ON information to the pixel. The voltage V_1 is positive at this time; however, it is decreased significantly due to the influence of the jump-in voltage. For example, the

select pulse is 10V and the voltage of the signal line is ± 8V. The jump-in voltage is to be half of the select pulse, namely 5V. Therefore, V_1 is 3V or equal to or less than that if sufficient charging is not realized during the duration time of the select pulse.

[0079]

Tr_2 is a depletion type of NMOS, thus, it is ON if V_1 is positive. Thereafter, the positive voltage is applied to the voltage supplying line and the pixel electrode is charged to be positive immediately since Tr_2 is in an ON state.

The voltage of the voltage supplying line becomes 0 before the next select pulse comes, and the voltage at the pixel electrode becomes 0 immediately. Next, it is supposed that the negative voltage is applied to the signal line as indicated by a solid line. Then, the value of V_1 becomes negative. With the influence of the jump-in voltage, the voltage of -13V is applied, and Tr_2 is in an OFF state. Accordingly, the pixel is not charged when the negative voltage is supplied to the voltage supplying line.

[0080]

If the positive voltage is supplied to the signal line continuously like a broken line, a positive signal is observed in V_1 as in the first cycle as indicated by a broken line. Thus, Tr_2 remains in an ON state, and thus, the pixel electrode is immediately charged by the negative voltage supplied by the voltage supplying line.

[0081]

Fig. 7 illustrates the case of CMOS. NMOS is used as Tr_1 and PMOS is used as Tr_2, but this configuration may be also inverted.

An example for an operation thereof is shown in the lower part in Fig. 7. Here, in the voltage indication of the signal line V_D, a positive signal is OFF and a negative signal is ON. At first, in order to transmit OFF information to the pixel, the voltage of the signal line is to be positive when the pulse of the select line is applied as indicated by a solid line. At this time, the voltage V_1 is positive; however, it is significantly decreased by the influence of the jump-in voltage. For example, the select pulse is to be 10V and the voltage of the signal line is ±8V. In addition, the jump-in voltage is half of the select pulse, namely 5V. Therefore, V_1 is 3V or equal to or less than that if sufficient charging is not realized during the duration time of the

select pulse.

[0082]

If V_1 is positive, Tr_2 is in an OFF state since it is PMOS. Thereafter, the positive voltage is applied to the voltage supplying line, however, the pixel electrode is not charged because Tr_2 is in an OFF state.

The voltage of the voltage supplying line becomes 0 before the next select pulse comes. Next, it is supposed that the negative voltage is applied to the signal line as indicated by a solid line. Then, the value of V_1 is negative. The voltage of -13V is applied with the influence of the jump-in voltage, and Tr_2 is in an ON state. Accordingly, the negative voltage is supplied to the voltage supplying line and the pixel electrode is immediately charged by this voltage.

[0083]

If the pixel is to be in an ON state for the two cycles, the voltage is applied to the signal line as depicted with a broken line. Namely, V_1 is a negative signal in each cycle as indicated by a broken line and Tr_2 remains in an ON state. Accordingly, the voltage supplied to the voltage supplying line charges the pixel electrode to make it positive in the first cycle and negative in the second cycle.

[0084]

An example of a signal for performing digital grading in accordance with the invention will be explained with reference to Fig. 8. As a circuit, a CMOS type as shown in Fig. 7, in which NMOS is used as Tr_1 and PMOS is used as Tr_2, is employed. An example of Fig. 8 shows the case of 32 grades-display but a display of a greater number of grades than 32 can be realized as a matter of course. Details of this technique are described in an invention of Japanese Patent Application No.Hei3-209869 by the same inventor or other.

[0085]

Several techniques are given for realizing digital grading. In order to lower the load on a driving equipment, the best technique is to realize and express a time for applying the voltage to a liquid crystal pixel by the sum of the plural pulses. In the example of Fig. 8, the shortest pulse width applied to the liquid crystal pixel is a 32nd of

33msec, namely around 1msec. This value is expressed as T_0 in Fig. 8. Of course, this time may be shorter to some extent. For example, the time is certainly shorter than the above in the case where the time for applying the voltage to the pixel is delayed so that Tr_2 operates evenly as described above, which is a feature of the invention. 70% to 90% of 1msec is sometimes used, for instance.

[0086]

However, the shortest repeating cycle of the pulse of the select line is a 32nd of one frame cycle (e.g., 33msec), and it is undesirable that the repeating cycle is too short or too long.

[0087]

In Fig. 8, after the first pulse is applied to the select line and T_0 seconds are passed, the pulse is applied again. Periods of the pulses applied to the select line are changed from $16T_0$, $2T_0$, $8T_0$ to $4T_0$ in order to complete one frame. The pulse width of the select line is determined in accordance with the number of rows of LCD matrix. If the number of rows is 480, the shortest time for one row is 2 μsec; however, it is selected to be 1 μsec for the purpose of avoiding overlapping pulses. This is a quite high speed as compared with that of the analog display technique of 30 to 70 μsec which is normal conventionally. Although such a high speed operation is required, there arises no problem since the load is significantly light as compared with that in the conventional technique, which is also a feature of the invention. Note that the pulse of the select line is to be 10V high.

[0088]

On the contrary, a positive or a negative signal is inputted to the signal line. If a positive signal is inputted, the voltage applied to the pixel is to be 0, whereas the pixel is to be in a voltage state if a negative signal is inputted. The voltage of a signal applied to the signal line is set at ±8V.

[0089]

As Tr_1, a transistor having a low quality is used; namely, change of the jump-in voltage (voltage drop) is 25% of the gate voltage and the voltage is reduced to 90% after time T_0 is passed (50%, after time $16T_0$ is passed). This quality is quite low and

the transistor cannot be used in an LCD of a conventional TFT system, however, can be utilized sufficiently in the invention as will be described hereinafter.

[0090]

As indicated by V_1 in Fig. 8, the voltage of Tr_1 at the source side is positive during the first T_0 and the next $16T_0$, but is negative during the following $2T_0$ and $8T_0$. During the last $4T_0$, the voltage is positive again.

[0091]

On the other hand, a pulse signal synchronized with the select line is sent to the voltage supplying line so that the duration time is in proportion to the period of the select pulse. For example, between the first select pulse and the next select pulse, the pulse of the voltage supplying line is started after 10μsec of the completion of the select pulse and is finished before 10μsec of the start of the next select pulse. Further, it may be started after 160μsec of the completion of the second select pulse and may be finished before 160μsc of the start of the third select pulse. The duration time of each pulse is expressed by a favorable ratio of the whole number.

[0092]

However, such a complicated step is not necessary and there is no problem actually in a step in which it is started simply after a predetermined time of the completion of the select pulse and is finished before a predetermined time of the start of the next select pulse.

[0093]

For example, the pulse of the voltage supplying line is started after 10μsec of the completion of the select pulse, and is finished after 10μsec before the start of the next select pulse. In that case, the duration time of the first pulse of the voltage supplying line is 0.98 msec and the duration time of the next pulse is 15.8 msec. The ratio thereof is 1:16.12, which is different from the ideal ratio of 1:16; however, the difference is 12% of the shortest pulse width, thereby providing no problem for 16 grades-display. Accordingly, the latter step is employed here as shown in Fig. 8.

[0094]

It is of course possible to perform an alternating display by inverting the pulse

of the voltage supplying line for each frame.

It is desirable to maintain electric potential of the opposed electrode to be grounding level at all times. The voltage at the pixel electrode is determined by V_1 and V_{LC}, and in the first two periods, namely T_0 and $16T_0$, V_1 is positive so that the voltage V_2 at the pixel is 0. In the following periods $2T_0$ and $8T_0$, V_1 is negative so that V_2 is in a voltage state; however, V_2 is 0 again in the last $4T_0$.

[0095]

During $31T_0$ (31μsec), a voltage state is generated for $10T_0$ (10μsec) and a 11 grades-display out of 32 grades can be realized (there is no voltage state in the first grade). In this way, in accordance with the invention, digital grading can be performed accurately.

[0096]

In the invention, the number of matrix columns is the same as in the conventional technique, but the number of rows is larger by the voltage supplying line. For coupling to the driver circuit, it is almost impossible to couple in the uniform manner as in a coupling by conventional TAB, and thus, it is necessary to use a special coupling technique. If a TFT is formed of a polysilicon TFT of a self-alignment manner, a peripheral circuit such as a driver can be also formed at the same time when the driving circuit of the pixel is formed, and therefore, it is unnecessary to concern about yield decrease due to coupling of each wiring.

[0097]

However, if an amorphous silicon TFT or a polysilicon TFT of not a self-alignment manner is used, a driver IC has to be connected to each terminal in addition. If a fine grading display such as 256 grades is performed, a driver operation with high speed is required even with a polysilicon TFT of a self-alignment manner. In such a case, even a polysilicon TFT cannot drive, and an external driver IC must be provided.

[0098]

In that case, as shown in Fig. 9, a driver IC 904 connected to the select line is provided on the left side of a panel 901 and a driver IC 905 connected to the voltage

supplying line is provided on the right side of the panel. Coupling of each wiring may be completed by exposing only the terminal of the select line on the left side and exposing only the terminal of the voltage supplying line on the right side.

[0099]

In Fig. 9, a matrix 902 is divided into two portions, top and bottom. A driver IC 03 connected the signal line is coupled to the top and the bottom of the panel respectively. In this way, two independent panels are provided in appearance so that the number of wirings of the select line and the voltage supplying line in each panel can be reduced by half. Therefore, the width of the select pulse is enlarged, which is particularly advantageous to perform a fine grading display.

[0100]

In order to implement the present invention, a known technique for manufacturing a TFT can be used. Details are explained in the following embodiments.

[0101]

[Embodiments of the Invention]

[Embodiment 1]

Fig. 10 and Fig. 11 show a technique to connect each electrode by a metal wiring under a condition where two TFTs have been provided for one pixel in advance. Fig. 10 illustrates a cross-sectional view of the manufacturing process and Fig. 11 illustrates a top view (view from a top direction) of the manufacturing process. The TFTs formed in advance may be the same type of TFTs or the different types of TFTs such as PMOS and NMOS TFTs or depletion type and enhancement type TFTs. In the figure, a planer type TFT is shown; however, any one of stagger type, inverted stagger type or the one having impurity regions (source, drain) formed by a self-alignment manner or a non-self-alignment manner can be used.

[0102]

When analog grading, digital grading or the like is performed by the conventional technique, it is desirable to employ a self-alignment manner since a parasitic capacitance of a TFT is a problem. Highly fine mask alignment technique is

utilized to reduce the parasitic capacitance in an amorphous silicon TFT since a self-alignment manner cannot be employed. However, in the present invention, even if the parasitic capacitance exists to some extent, or rather, by the parasitic capacitance, effective operation is sometimes possible, which is a feature of the invention as described above. Of course, it is desirable that the parasitic capacitance is smaller because the load on the peripheral circuit is lowered.

[0103]

Fig. 10(A) and Fig. 11(A) show a condition where a TFT is manufactured. Here, it is shown that two TFTs, 107 and 108, are already formed. Reference numeral 101 denotes a substrate of glass or the like, 102 denotes a blocking layer which can block movable ions such as sodium ions from entering a TFT from the substrate, and silicon nitride, aluminum oxide or the like is preferably used to form this layer.

[0104]

Reference numeral 103 denotes an insulating film formed from silicon oxide or the like which is formed in order to hinder formation of an interfacial state between the blocking layer and a semiconductor of the TFT. Reference numeral 104 denotes a semiconductor coating film, and an impurity region is formed therein because a planer manner is employed in the figure. The thickness of the coating film is preferably 20 to 100 nm. This coating film is desired to be finally polysilicon if a self-alignment manner is employed. Reference numeral 105 denotes an insulating film which functions as a gate insulating film, and a silicon oxide film formed by sputtering or ECR-CVD is preferable for the purpose. The thickness is preferably in a range of 50 to 200 nm. Reference numeral 106 denotes a gate electrode. It is preferably formed of a semiconductor material such as silicon doped with a concentrated impurity or a refractory metal such as chromium or tungsten in order to achieve the purpose if a self-alignment manner is employed to introduce an impurity. Further, these gate electrodes are exposed in steps of Fig. 10 (A) and Fig. 11(A).

[0105]

Next, a hole is opened for a source region and a drain region of a TFT 107 as shown in Fig. 10(B) and Fig. 11(B), and a metal coating film is formed and etched to

connect the drain region to a signal line 110. At the same time, the source region is connected to the other TFT, namely the gate electrode 108, by a metal wiring 109. Here, the gate electrode of the TFT 108 is exposed, and thus, it is unnecessary to open a hole.

[0106]

Then, an interlayer insulating film 111 is formed. As shown in Fig. 10(C) and Fig. 11(C), a hole is opened for the gate electrode of the TFT 107 and for the drain region of the TFT 108. Thereafter, a metal coating film is formed to connect the gate electrode of the TFT 108 to the signal line 103 and to connect the drain region of the TFT 108 to the voltage supplying line 112. The interlayer insulating film is particularly desired to have a favorable insulating property for the invention because an electric charge is desirably maintained at the gate electrode of the TFT which functions as Tr_2 during one frame. It is not necessary that there is no leak of an electric charge, but too large leak can be a serious problem for the invention.

[0107]

A surface smoothing film 114 is formed finally. As shown in Fig. 10(D) and Fig. 11(D), a hole is opened for the source region of the TFT 108, then, a pixel electrode and a wiring thereof 115 are formed of a transparent conductive material such as an ITO (an alloy of indium oxide and tin oxide). According to the above process, a pixel to implement the invention can be manufactured.

[0108]

[Embodiment 2]

Fig. 12 shows the present embodiment. Fig. 12 is a cross-sectional view explaining an example of the present invention using two inverted stagger type TFTs.

[0109]

As shown in Fig. 12(A), inverted stagger type TFTs 209 and 210 are formed on a glass substrate 201. Reference numeral 202 is a blocking layer for blocking movable ions from entering from the substrate and is preferably formed of silicon nitride or the like. Further, reference numeral 203 denotes a gate electrode formed of a metal such as aluminum or a semiconductor material such as silicon. When the yield is intended

to be improved by employing a low temperature process, aluminum having the low conductivity can be selected. When aluminum is used, a gate electrode of the TFT 209 among these gate electrodes is preferably formed with the select line already connected thereto in patterning. On the other hand, a gate electrode of the TFT 210 is electrically insulated. Additionally, an oxide film of 10 to 30 nm thick may be formed on a gate electrode surface by anodic oxidation or other method.

[0110]

Reference numeral 204 is a gate insulating film, which can preferably function as an interlayer insulating film. As an activated region of a TFT, an I type amorphous silicon film 205 is formed for the TFT 209 and an N type amorphous silicon film 206 is formed for the TFT 210. Polysilicon may be also used instead of amorphous silicon. In both TFTs, an N^+ type microcrystalline silicon film 207 is formed by using an etching stopper 208, thereby providing a source and a drain. According to the above structure, the TFT 209 functions as an enhancement type TFT and the TFT 210 functions as a depletion type TFT.

[0111]

If the circuit as shown in Fig. 7 is constituted to provide a CMOS type, both the activated regions (205 and 206) are formed from an I type, and the source and the drain are formed from a P type and an N type. Since the mobility in a P channel TFT using amorphous silicon is very low, polysilicon is more preferably used in order to provide a CMOS type. However, unless a particular method such as laser annealing is employed, it is difficult to manufacture polysilicon at a low temperature, which is also the case in the depletion type. For example, when aluminum is used to form the gate electrode, attention must be paid because aluminum tends to be degraded at a process temperature of 550 °C or more.

[0112]

In the step of Fig. 12(A), the gate electrode of the TFT 210 has no electric contact to outside due to the interlayer insulating film 204.

As illustrated in Fig. 12(B), a metal coating film is formed and patterned to connect the drain of the TFT 209 to the signal line 211, whereas a hole is opened for the

gate electrode of the TFT 210 and a metal wiring 212 is formed to connect the source of the TFT 209 to the gate of the TFT 210.

[0113]

Further, after an interlayer insulating film 213 is formed, a hole is opened for the drain of the TFT 210, and a metal wiring 214 connected to the voltage supplying line is formed as illustrated in Fig. 12(C).

Finally, after a surface smoothing film 216 is formed, a pixel electrode 217 is formed by a transparent conductive material (Fig. 12(D)), and thus, manufacture of a pixel for the invention is completed.

[0114]

[Embodiment 3]

The present embodiment is shown in Fig. 13. Fig.13 is top views describing an example of the invention using two inverted stagger type TFTs.

As illustrated in Fig. 13(A), on a glass substrate, a metal wiring 301 which functions as a select line and a gate electrode of the first TFT and a metal wiring 301' which functions as a gate electrode of the second TFT are provided. These wirings are formed by patterning of the same coating film. Before patterning, an oxide film of 10 to 30 nm thick may be preferably formed on the metal coating film surface by anodic oxidation or other method.

[0115]

Further, after the gate insulating film which also functions as an interlayer insulating film is formed, a semiconductor coating film 302 is provided. In addition, a contact hole 304 is formed for the gate electrode of the second TFT, and then, a concentrated impurity-doped semiconductor film 305 as source and drain electrodes of the first TFT and a concentrated impurity-doped semiconductor film 303 as source and drain electrodes of the second TFT are formed. These two semiconductor coating films 303 and 305 may be formed of the same material, the same coating film, the same conductivity type or the different conductivity type. CMOS type can be formed if the different conductivity type is employed.

[0116]

In addition, a portion of the semiconductor coating film 305 which functions as a source of the first TFT is connected to the gate electrode of the second TFT through the contact hole 304. Fig. 13(A) is obtained like this.

As illustrated in Fig. 13(B), a metal coating film is formed and patterned in order to connect the drain of the first TFT to a signal line 306. After the interlayer insulating film is provided, the drain of the second TFT is provided with a contact hole 307 and the source thereof is provided with a contact hole 309, and connected to a voltage supplying line 308 and a pixel electrode 310 respectively as shown in Fig. 13(C). Thus, manufacture of a pixel for the invention is completed.

[0117]

The above described steps to form the CMOS type circuit are summarized as follows. The numbers in brackets [ ] are the number of masks.

(1) formation of the select line 301 and the gate electrode 301'[1],

(2) formation of the gate insulating film (interlayer insulating film),

(3) formation of the semiconductor layer 302[2],

(4) formation of the etching stopper (not shown)[3],

(5) formation of the contact hole 304[4],

(6) formation of the semiconductor layer 305[5],

(7) formation of the semiconductor layer 303[6],

(8) formation of the signal line 306[7],

(9) formation of the interlayer insulating film,

(10) formation of the contact holes 307 and 309[8],

(11) formation of the voltage supplying line 308[9],

(12) formation of the pixel electrode 310 [10].

Namely, the circuit is manufactured by ten mask processes.

[0118]

[Embodiment 4]

Fig. 14 shows an actual circuit example for the present invention. Fig. 14(A) is a cross-sectional view thereof and Fig. 14(B) is a top view thereof. This circuit is manufactured as follows.

[0119]

A wiring 402, which is a gate electrode of the first TFT and functions as a select line, is formed on a substrate 401. After formation of the wiring, an oxide film of 10 to 200 nm thick may be formed on a surface of the wiring by anodic oxidation or the like. The side surface of the gate electrode or the select line may be tapered as shown in the figure. By this tapered surface, the unevenness is avoided and the adhesiveness of the coating film which is laminated thereon is improved, further, fine processing can be performed with no problem.

[0120]

In particular, in the case where the gate electrode also serves as a select line as in this example, the width of the select line is required to be larger or the thickness is required to be larger in order to lower the resistance of the select line. However, for the purpose of maintaining the aperture ratio and shorten the channel length, there is a problem when the width of the select line is made larger. Accordingly, it is desired to enlarge the thickness of the select line. However, a coating film which is formed on the select line may be affected by the unevenness if the thickness of the select line is too large. Considering this, the tapered surface is preferable.

[0121]

A gate insulating film 403 is formed on the select line 402 (the gate electrode of the first TFT). This gate insulating film also serves as an interlayer insulating film, and after or during formation thereof, its surface is desirably smoothed by an etch back method.

[0122]

A coating film 405 of 20 to 100nm thick is formed as an activated semiconductor film of the first TFT on such a smooth gate insulating film. The film 405 is made of amorphous silicon, polysilicon or silicon having an intermediate state between them. A coating film such as silicon nitride is formed thereon and patterned as an etching stopper 406. It is particularly effective to provide such an etching stopper when a coating film in a lower layer is very thin as above and therefore tends to be cut in etching of the multilayer coating films of the same material. Furthermore, the

channel length of the TFT is substantially determined by the width of this etching stopper.

[0123]

Next, for example, an N^+ type microcrystalline silicon film is formed and patterned in order to provide a drain 408 of the first TFT and a wiring 407 which serves as both a source of the first TFT and a gate electrode of the second TFT. In accordance with the invention, an electric charge accumulated in the wiring 407 effects the operation property significantly. Therefore, as the wiring capacitance at this part is larger, the load on the first TFT (Tr_1) becomes heavier. In terms of a high speed operation, an arrangement to make a surface area as small as possible is desired, in addition, the invention provides more advantages if an integrated structure as in the present embodiment is formed.

[0124]

Then, a signal line 409 is formed from a metal material such as aluminum in this condition. Since the drain of the first TFT is exposed, sufficient contact is generated when just a metal wiring is formed to be overlapped thereon.

[0125]

Next, an insulating coating film 410 is formed. This film functions as a gate insulating film of the second TFT and further as an interlayer insulating film. Silicon oxide or the like is preferably used for a material of this film. As an activated semiconductor film 411, a coating film of polysilicon or silicon having an intermediate state between amorphous silicon and polysilicon is formed thereon. The thickness thereof is 20 to 100 nm. A coating film of silicon nitride or the like is formed thereon and patterned as an etching stopper 412.

[0126]

Next, for example, a P^+ type microcrystalline silicon film is formed and patterned in order to provide a source and a drain 413 of the second TFT. In this condition, these source region and drain region are exposed. Thus, favorable contact is generated by forming a voltage supplying line 414 from a metal material such as aluminum on the drain, or by forming a pixel electrode 415 from a coating film of a

transparent conductive material such as ITO on the source.

[0127]

The above steps are summarized as follows. The numbers in brackets [ ] are the number of masks.

(1) formation of the select line 402[1],

(2) formation of the gate insulating film (interlayer insulating film)403,

(3) formation of the semiconductor layer 405[2],

(4) formation of the etching stopper 406[3],

(5) formation of the semiconductor layers 407 and 408[4],

(6) formation of the signal line 409[5],

(7) formation of the gate insulating film (interlayer insulating film) 410,

(8) formation of the semiconductor layer 411[6],

(9) formation of the etching stopper 412[7],

(10) formation of the semiconductor layer 413[8],

(11) formation of the voltage supplying line 414[9],

(12) formation of the pixel electrode 415[10].

[0128]

Namely, the circuit can be manufactured by ten mask processes. A feature of the above technique is that the circuit can be provided without forming any contact hole. Coupling of a wiring by a contact hole causes sometimes breaking or bad electrical contact due to the unevenness of a hole; however, such a problem is not observed in this embodiment.

[0129]

[Effect of the Invention]

According to the present invention, the yield is significantly improved as compared with those of conventional analog grading or digital grading systems. Namely, even if an inferior TFT element which has been defined as defect in a conventional system is used, a sufficient grading display can be obtained from the above described reason. Accordingly, yield can be improved and the production cost can be reduced, which is a feature of the invention. It is also a feature of the invention that a

grading display with the same or higher quality than the conventional technique is achieved at the lower cost.

[0130]

When a polysilicon TFT manufactured by a self-alignment manner is used for two TFTs in the invention, LCD which is excellent in operation at high speed and in a fine grading display can be manufactured.

[0131]

Even if a polysilicon TFT manufactured by a non-self-alignment manner is employed for two TFTs, it is possible to display a graded image of 64 grades or more without any particular difficulty at a production cost which is no higher than or significantly lower than that of the conventional analog system LCD capable of displaying a 16 graded image.

[0132]

Also, even if an amorphous silicon TFT manufactured by a non-self-alignment manner is used for two TFTs, it is possible to manufacture large sized LCD capable of displaying 16 or more grades at a low cost.

[0133]

The present inventor believes that the invention can save the liquid crystal business field in an economic morass where no profit accounts are expected due to deficit, suffering from write-off cost of prior investment due to uncertain low yield and the high cost, and at the same time, the invention can develop a new applicable field which cannot be expected in a conventional expensive liquid crystal display, and can trigger a liquid crystal display market which significantly exceeds a conventional economic expectancy.

[Brief Description of the Drawings]

[Fig. 1] A circuit diagram and an operational diagram of a pixel of TFTLCD according to the present invention

[Fig. 2] A circuit diagram and an operational diagram of a pixel of a conventional TFTLCD

[Figs. 3] A circuit diagram and an operational diagram of a pixel of TFTLCD according

to the present invention

[Figs. 4] A circuit diagram and an operational diagram of a pixel of TFTLCD according to the present invention

[Fig. 5] A circuit diagram of a pixel of TFTLCD according to the present invention

[Fig. 6] A circuit diagram and an operational diagram of a pixel of TFTLCD according to the present invention

[Fig. 7] A circuit diagram and an operational diagram of a pixel of TFTLCD according to the present invention

[Fig. 8] A signal waveform diagram during a digital grading in accordance with the present invention

[Fig. 9] A mounting example figure of TFTLCD having the present invention

[Fig. 10] A figure showing a manufacturing method of a circuit according to the present invention

[Fig. 11] A figure showing a manufacturing method of a circuit according to the present invention

[Fig. 12] A figure showing a manufacturing method of a circuit according to the present invention

[Fig. 13] A figure showing a manufacturing method of a circuit according to the present invention

[Fig. 14] A figure showing a manufacturing method of a circuit according to the present invention

[Explanation of Reference Numerals]

104 Semiconductor coating film

106 Gate electrode

107 First TFT

108 Second TFT

109 Metal wiring

110 Signal line

112 Voltage supplying line

113 Select line

115 Pixel electrode

[Name of Document] Abstract

[Summary]

[Object]

Regarding an electro-optical display device such as an active matrix type liquid crystal display, a circuit formed of a pixel suitable for grading display (particularly, a digital grading display), driving method thereof and a manufacturing method thereof are provided, and image deterioration due to property dispersion between pixels is eliminated therein.

[Construction]

In an active matrix type flat panel display, a voltage supplying line is provided in addition to a select line and a signal line, and thus, a voltage state of each pixel is maintained almost constant by connecting each pixel to the voltage supplying line, thereby reducing a voltage variation between the pixels.

Particularly for this purpose, two transistors are provided in one pixel. A pixel is selected in the first transistor, a result of the selection is transmitted to the second transistor and a voltage added to the pixel is controlled in the second transistor.

Further improvement of the property is intended by combination of the first transistor and the second transistor in which the property is different from each other.

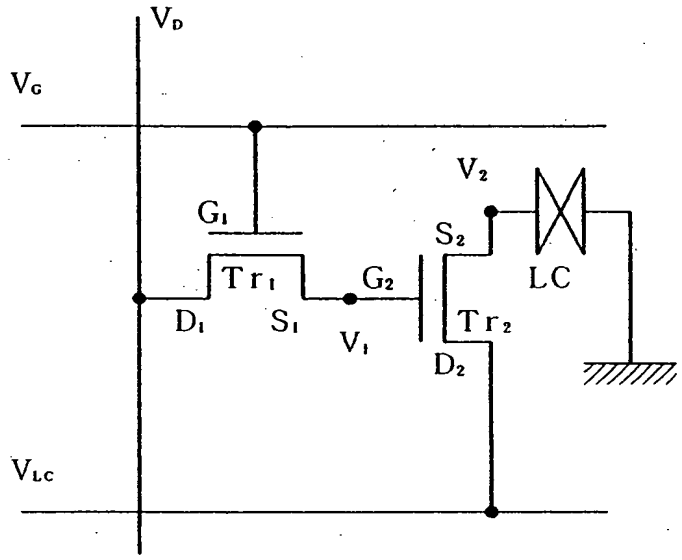
[Selected Drawing] Fig. 1

【整理番号】 P001991-01

【書類名】 図面

【~~図~~ 1】

Fig. 1



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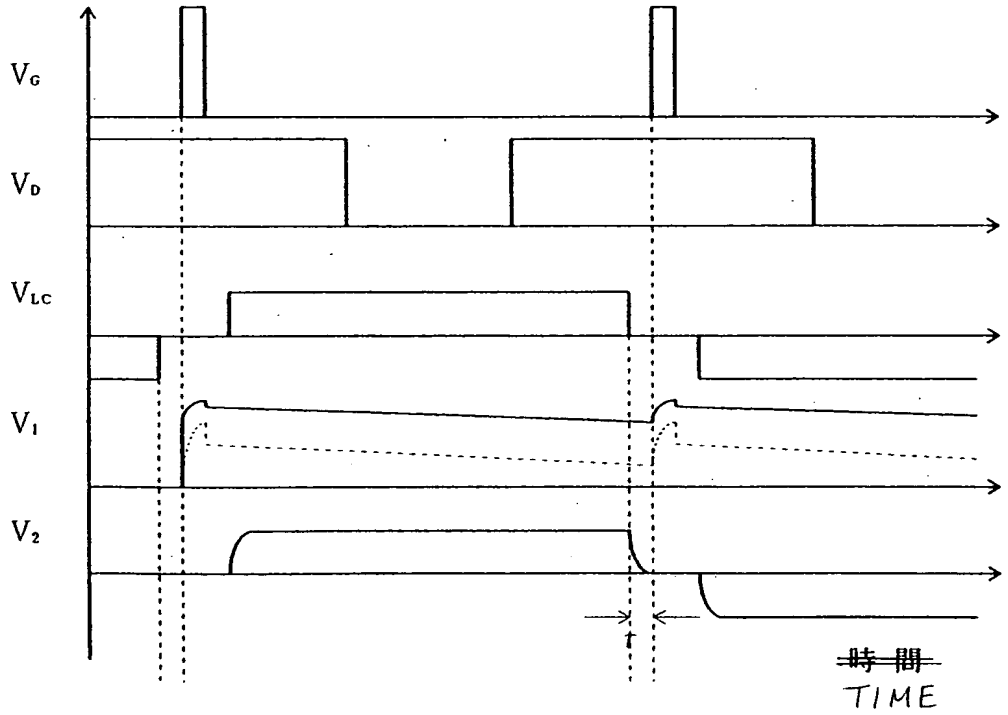

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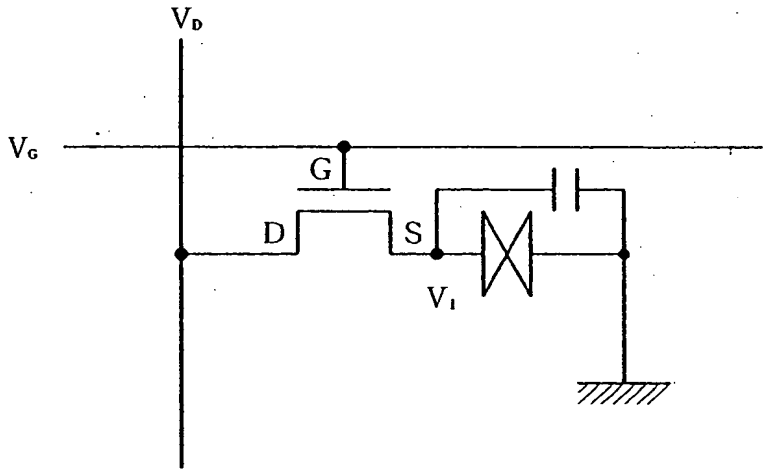
【~~図 2~~】
Fig. 2



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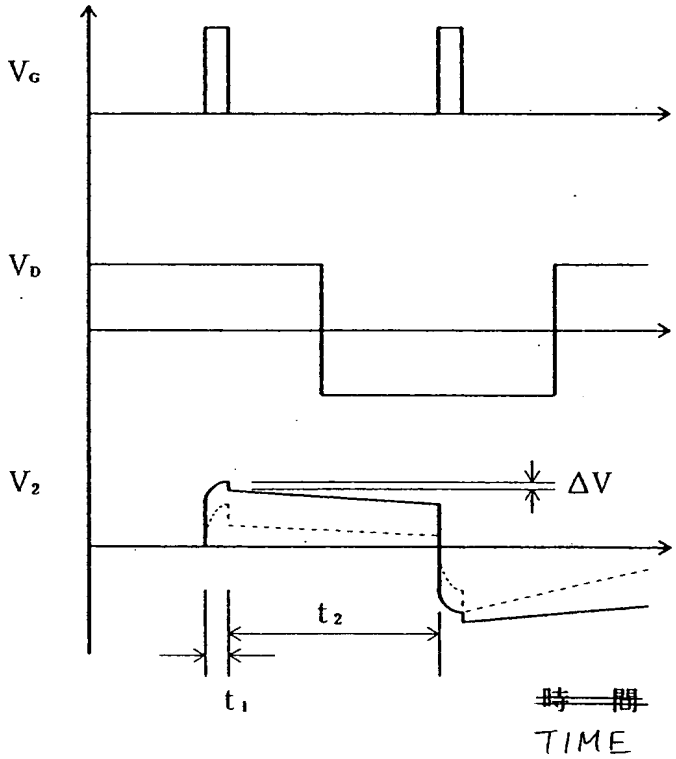

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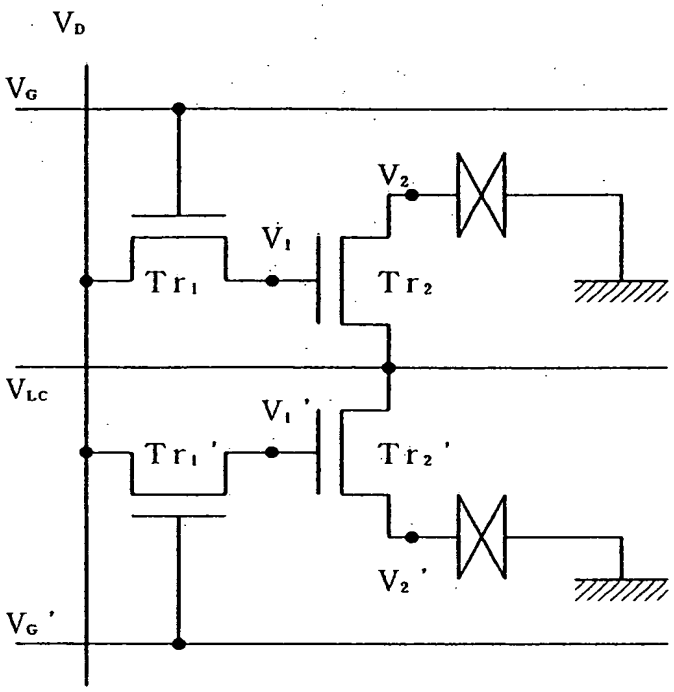
【~~図~~ 3】

Fig. 3



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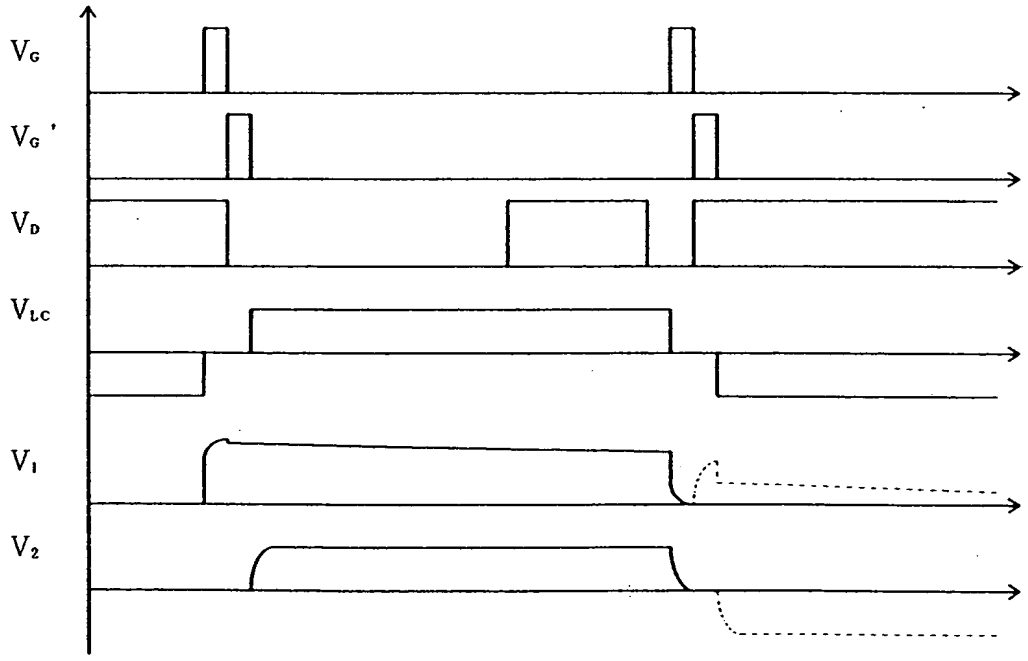

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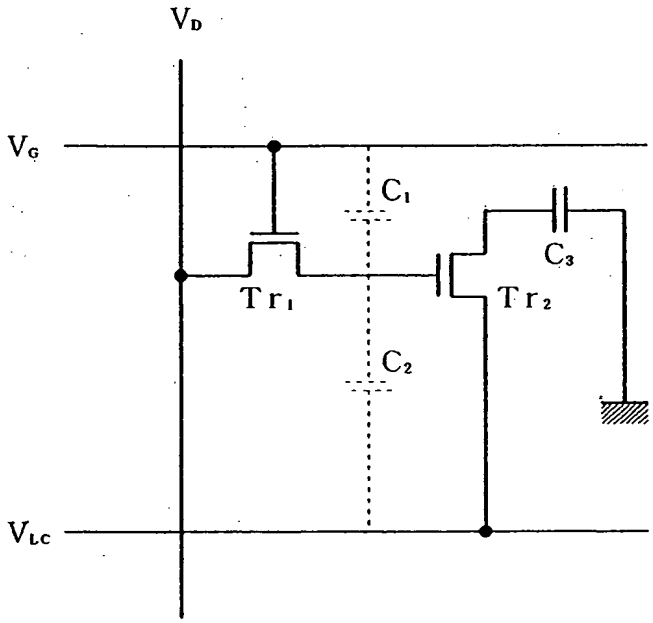
【~~図~~ 4】

Fig. 4



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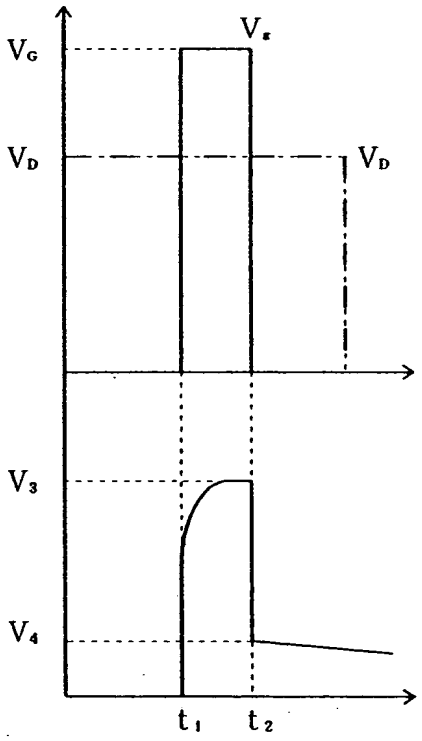

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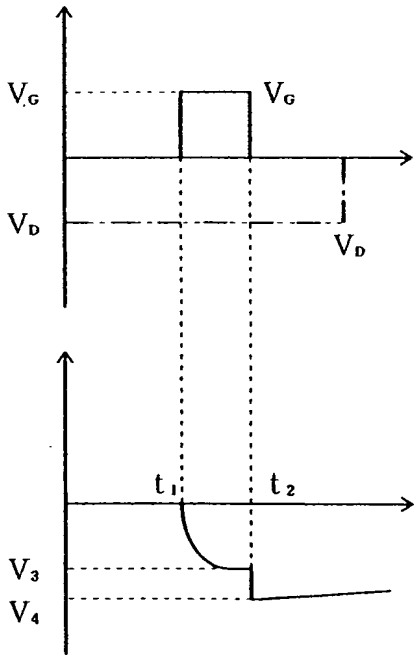

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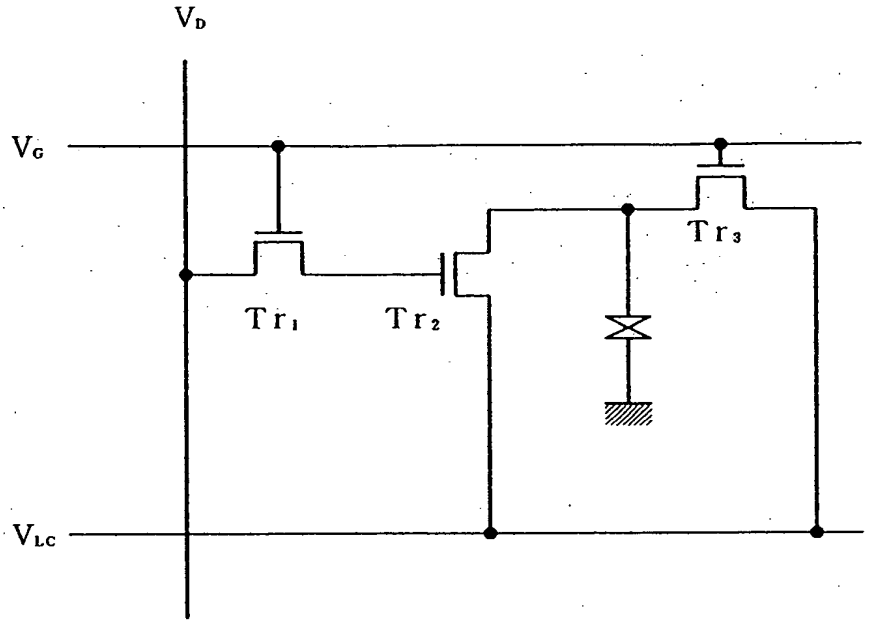
【~~図~~ 5】
Fig. 5

（A）



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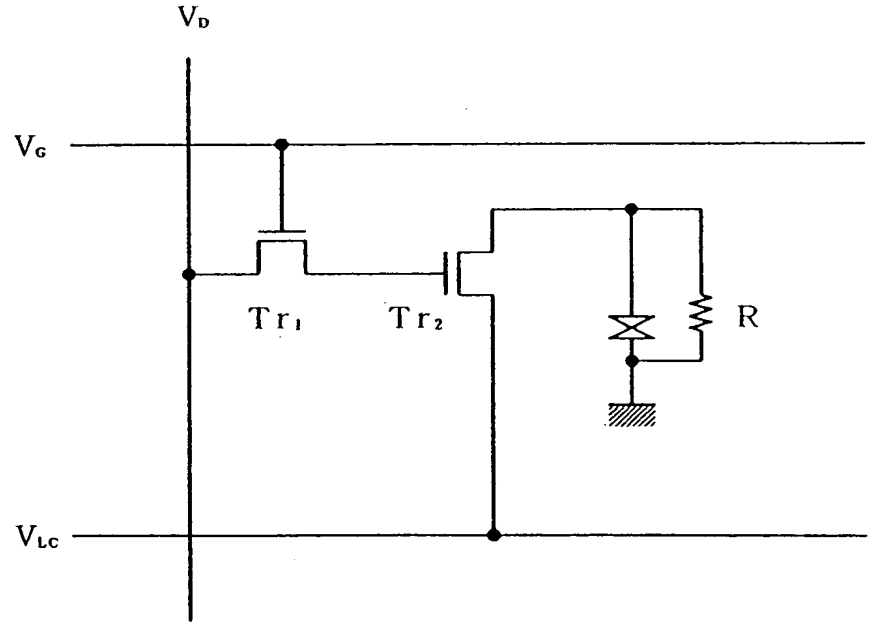

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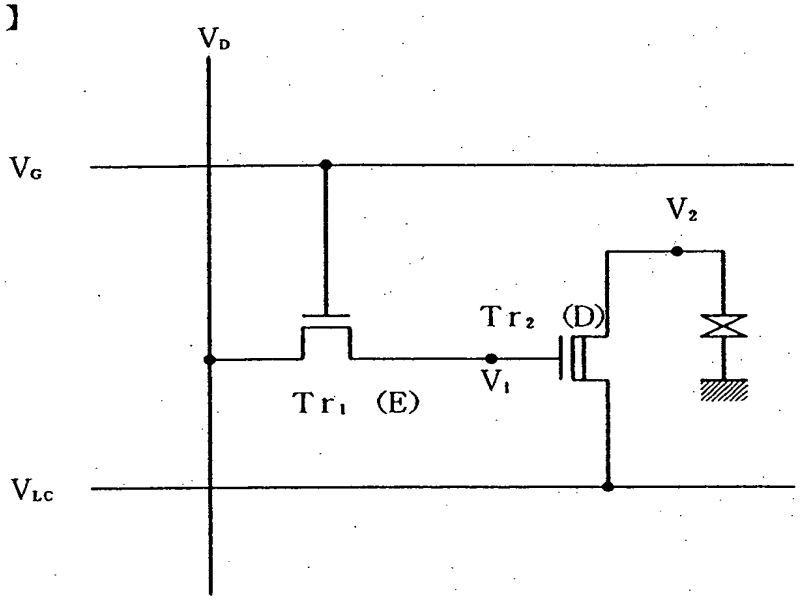
【~~図 6~~】

Fig. 6



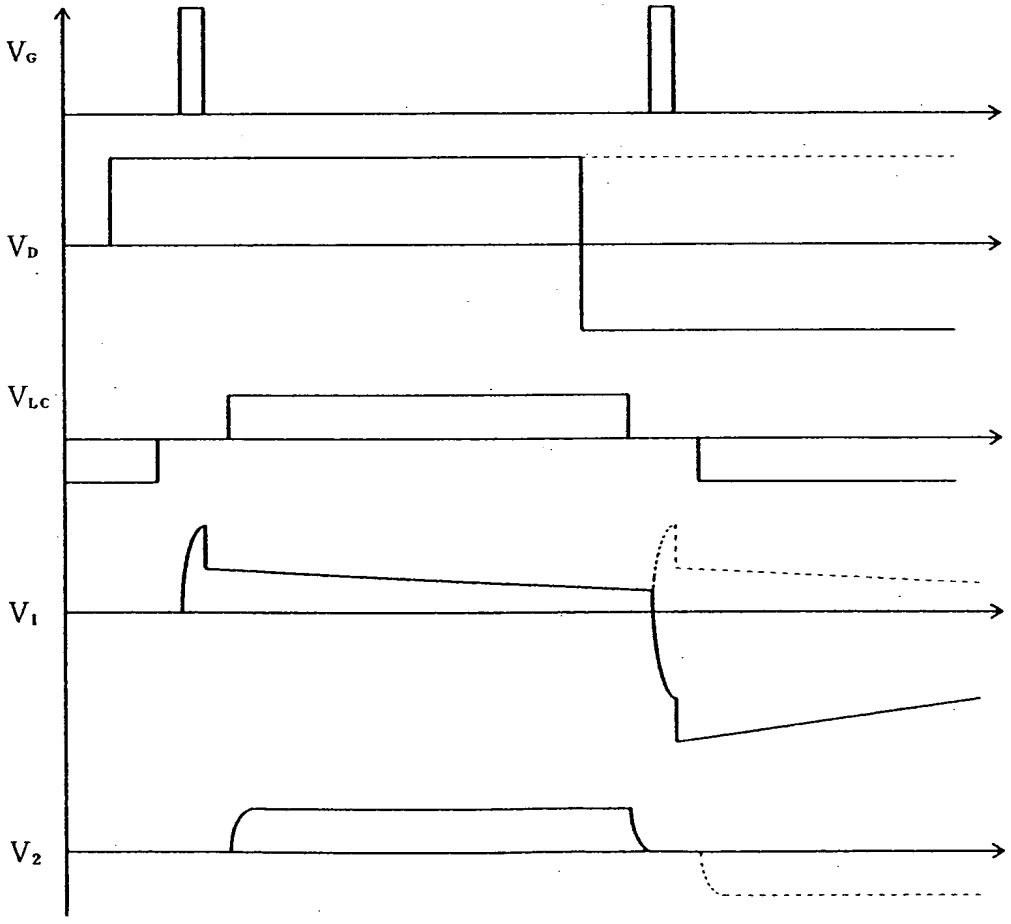


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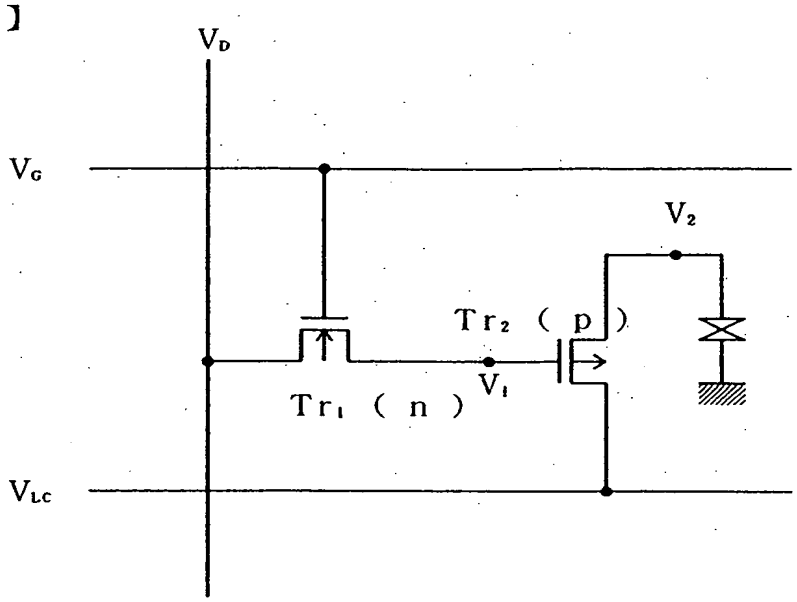
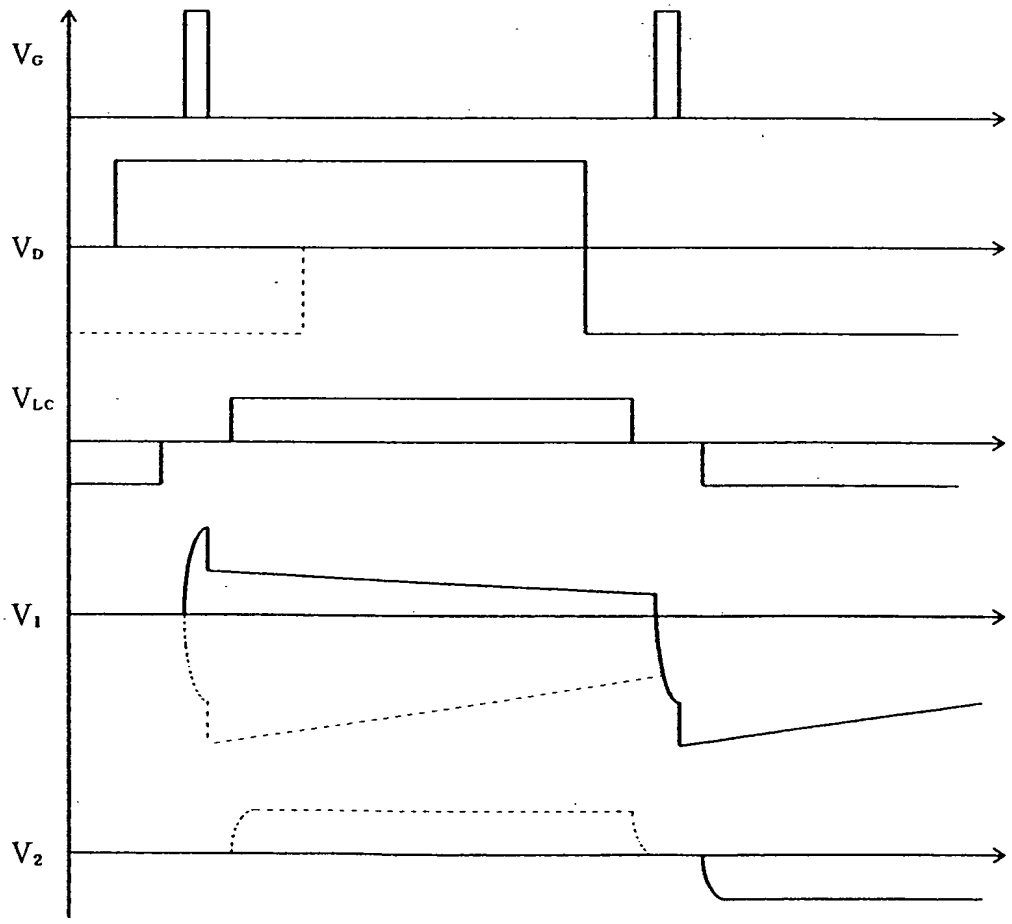
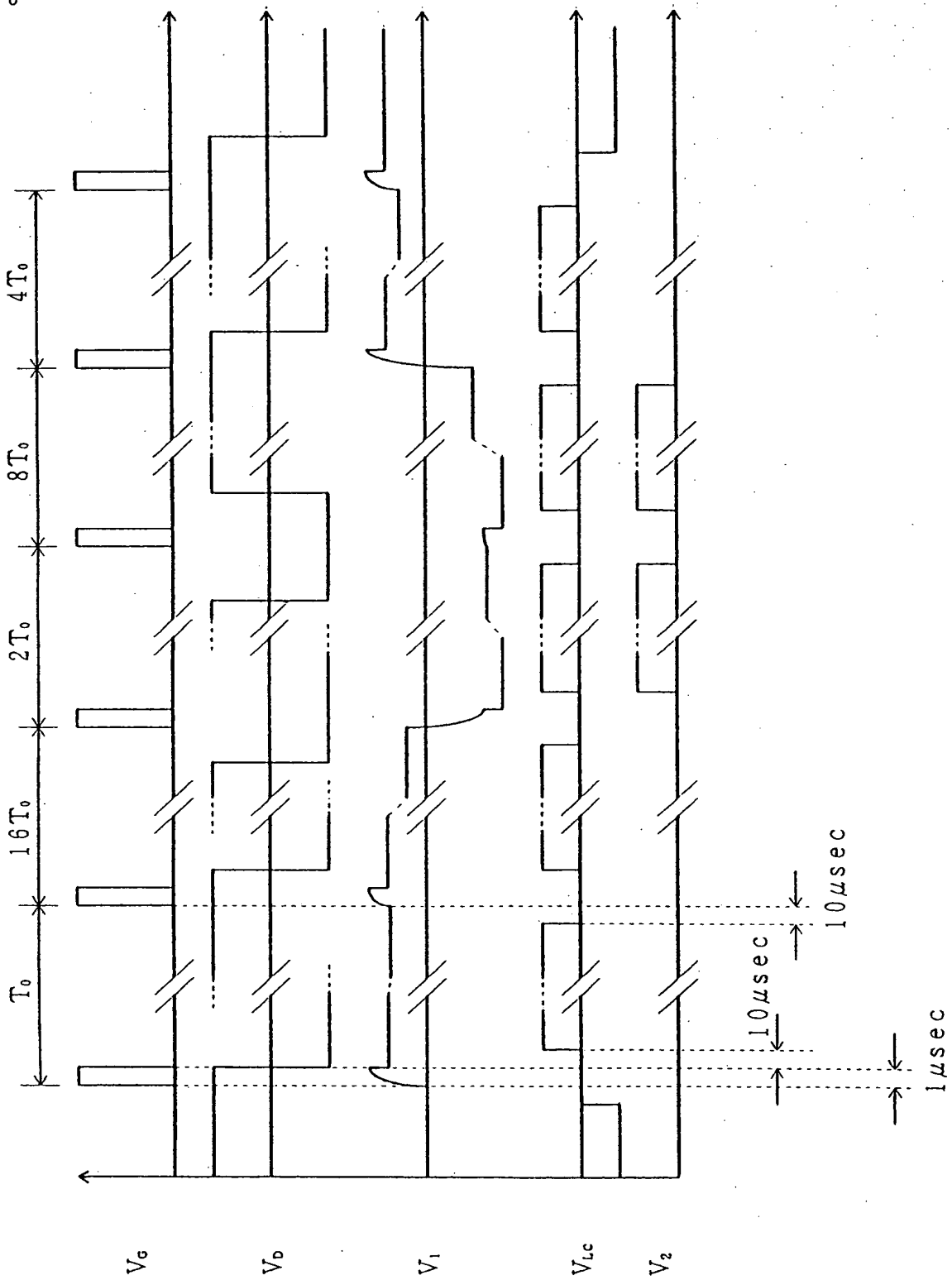
Fig. 7





【~~図 8~~】

Fig. 8



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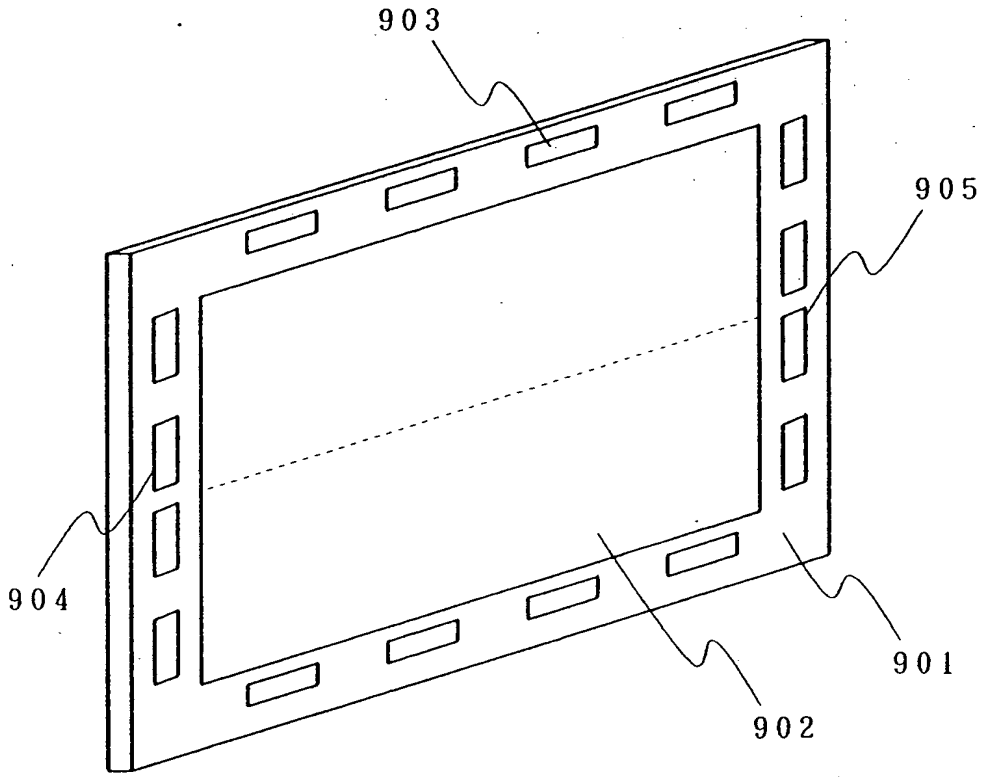
【~~図 9~~】
Fig. 9



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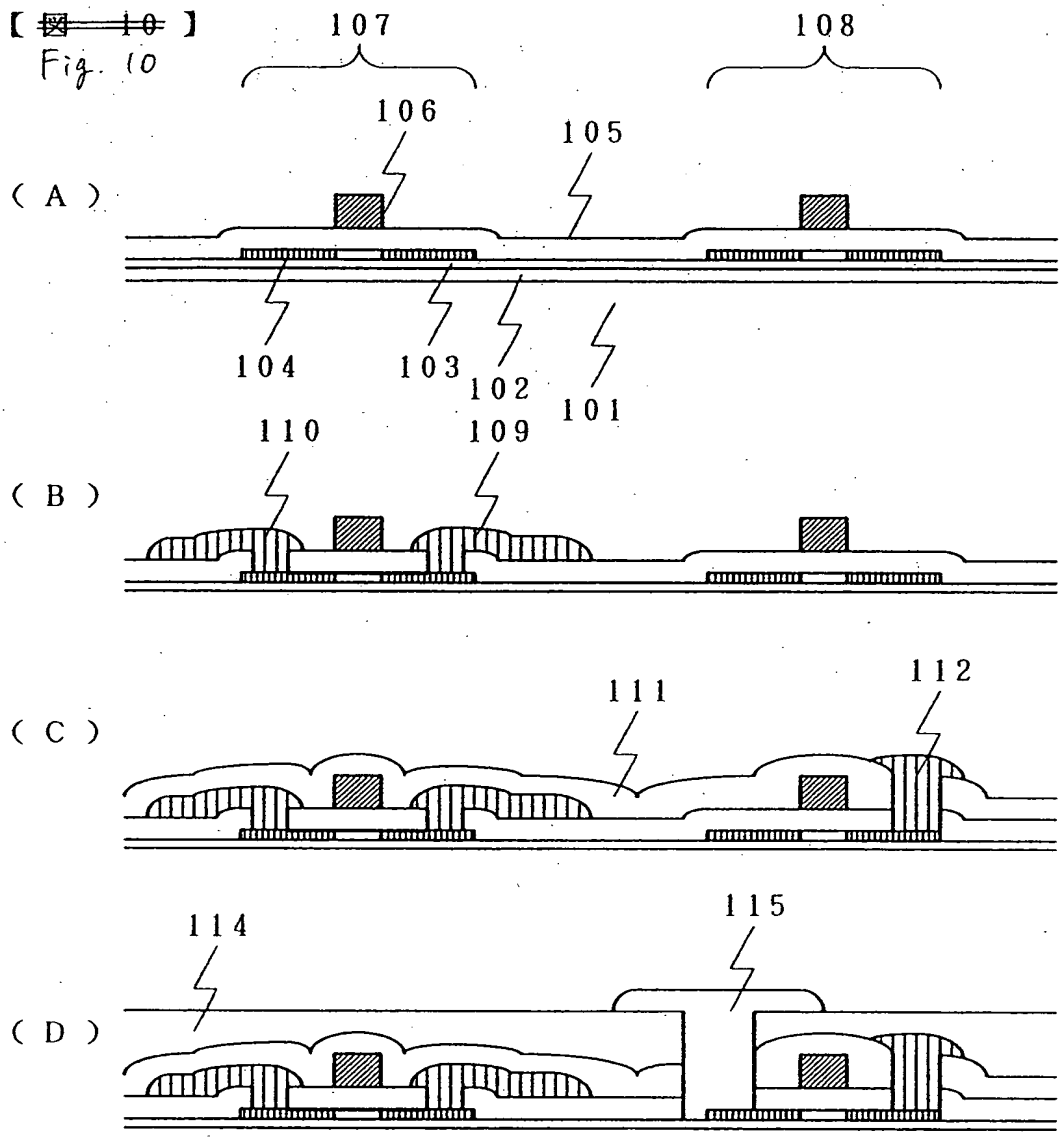
【~~図 10~~】
Fig. 10



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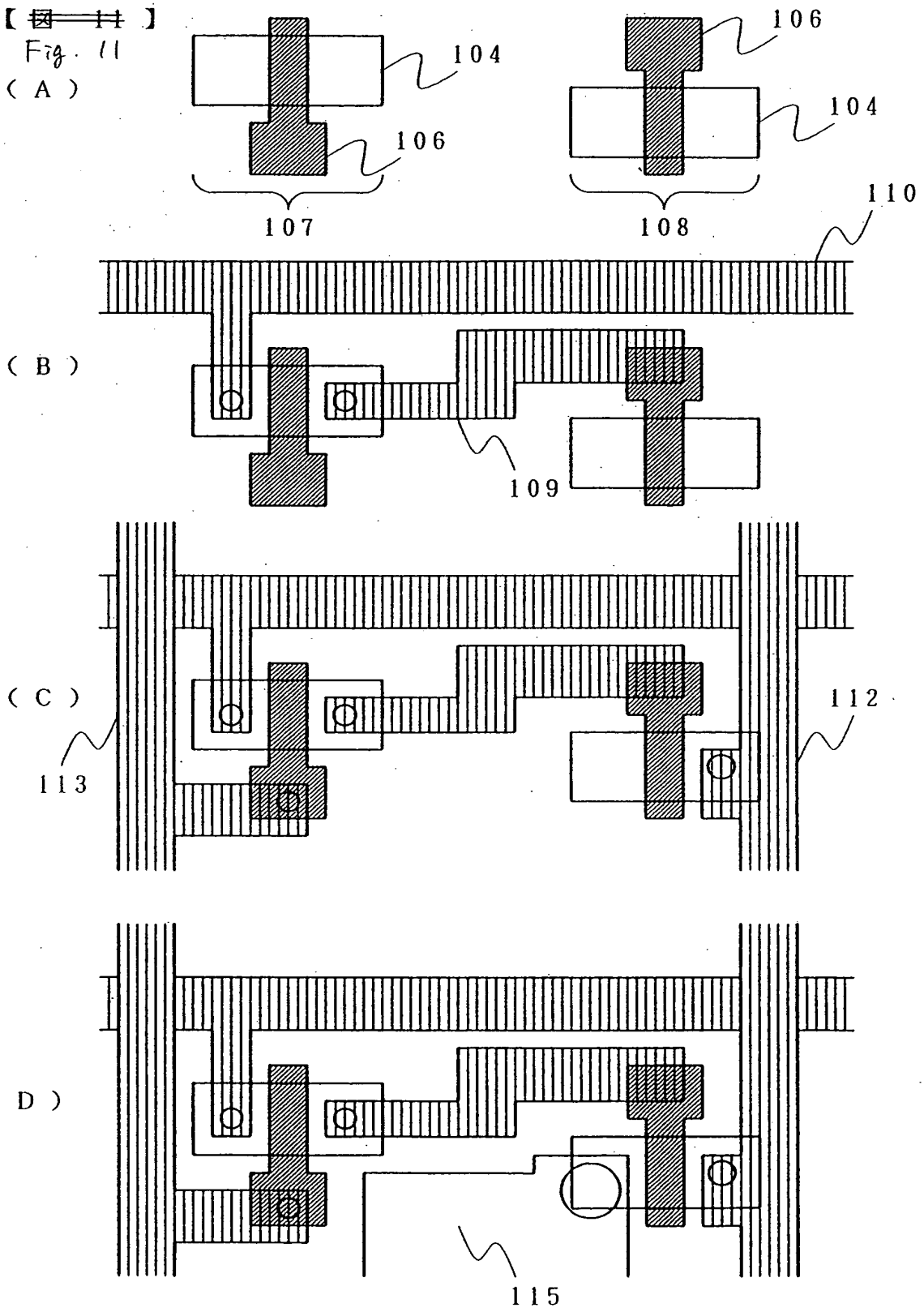
【~~図 11~~】
Fig. 11



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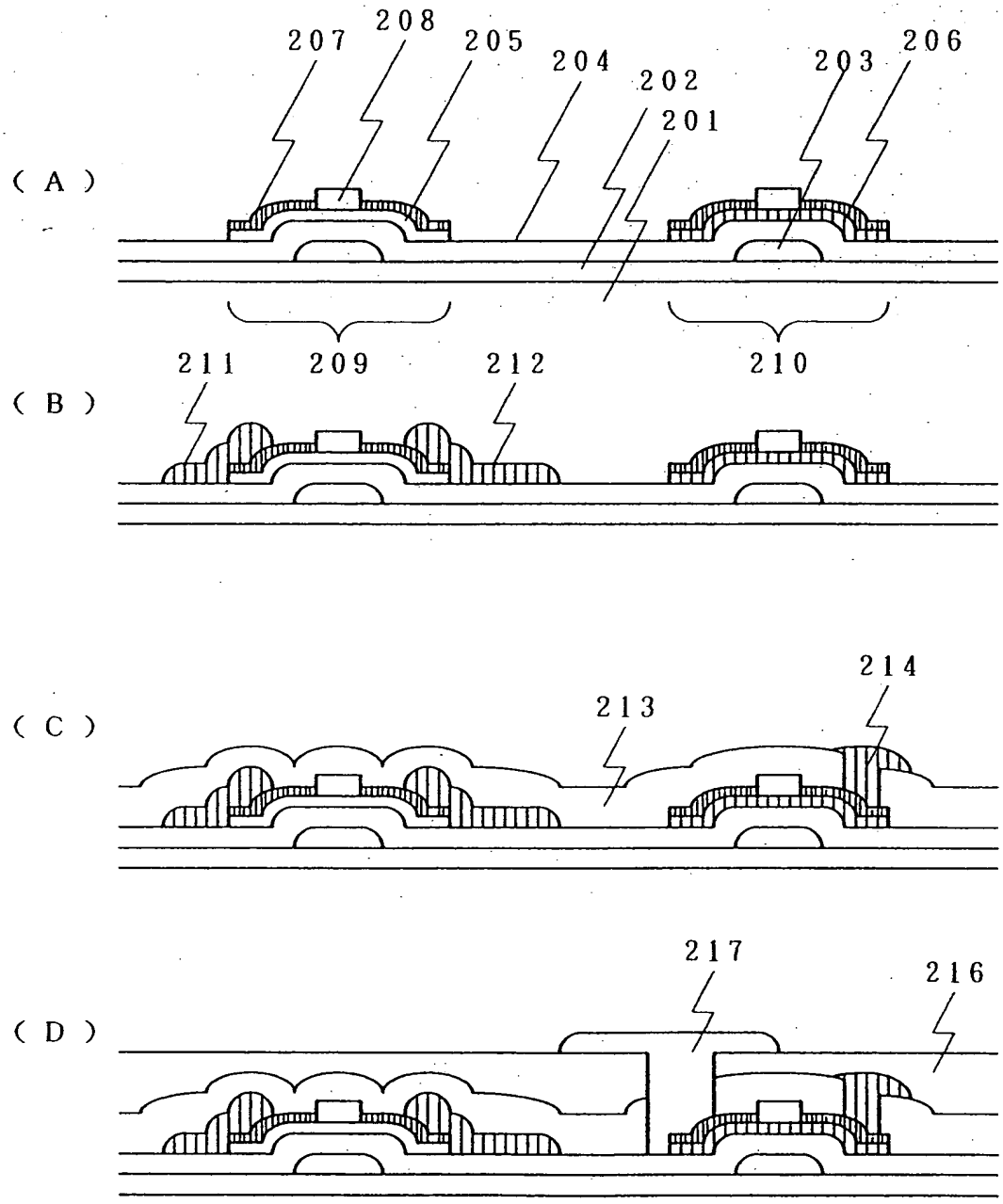
【~~図 12~~】
Fig. 12



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【~~図 13~~】
Fig. 13

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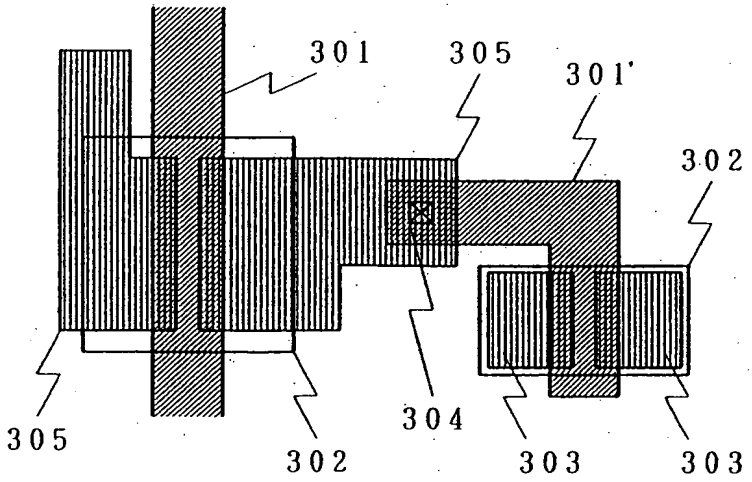

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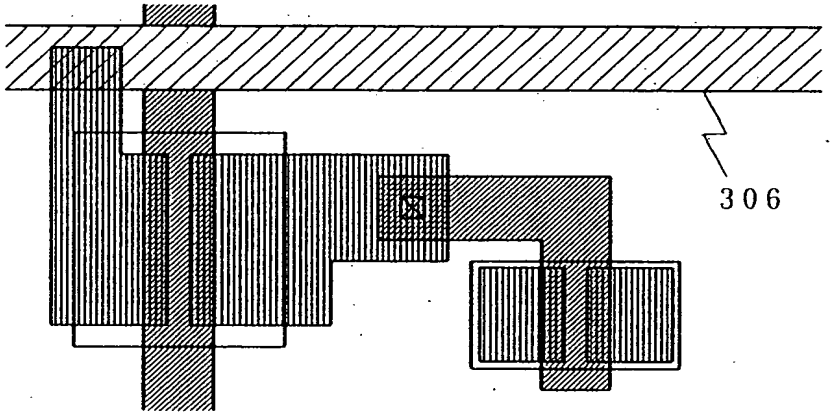

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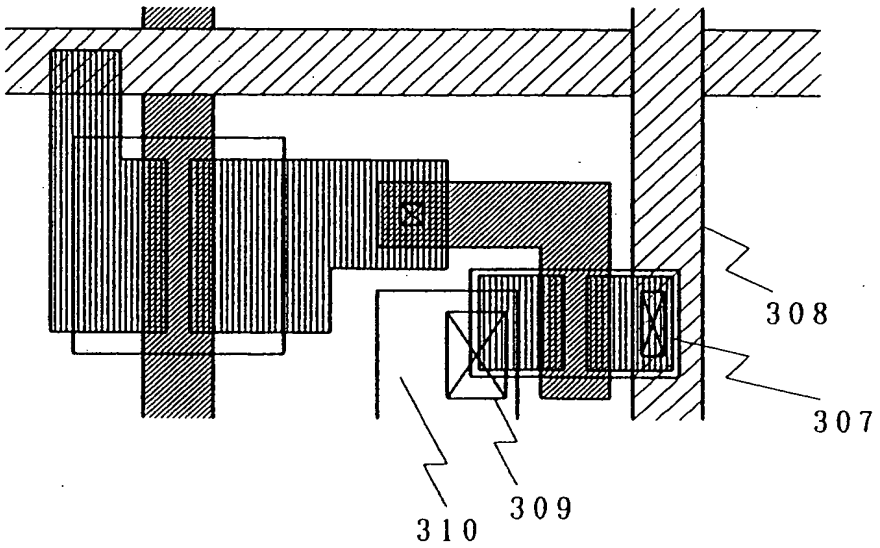

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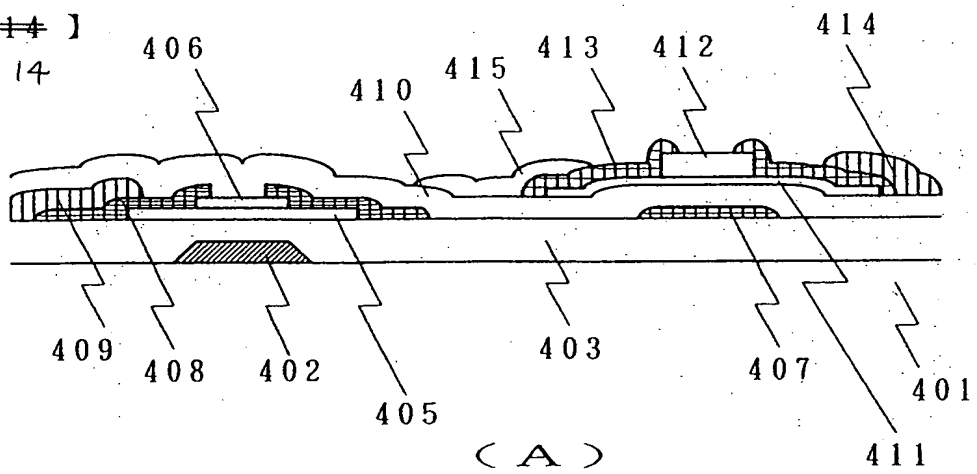
【~~図 14~~】

Fig. 14



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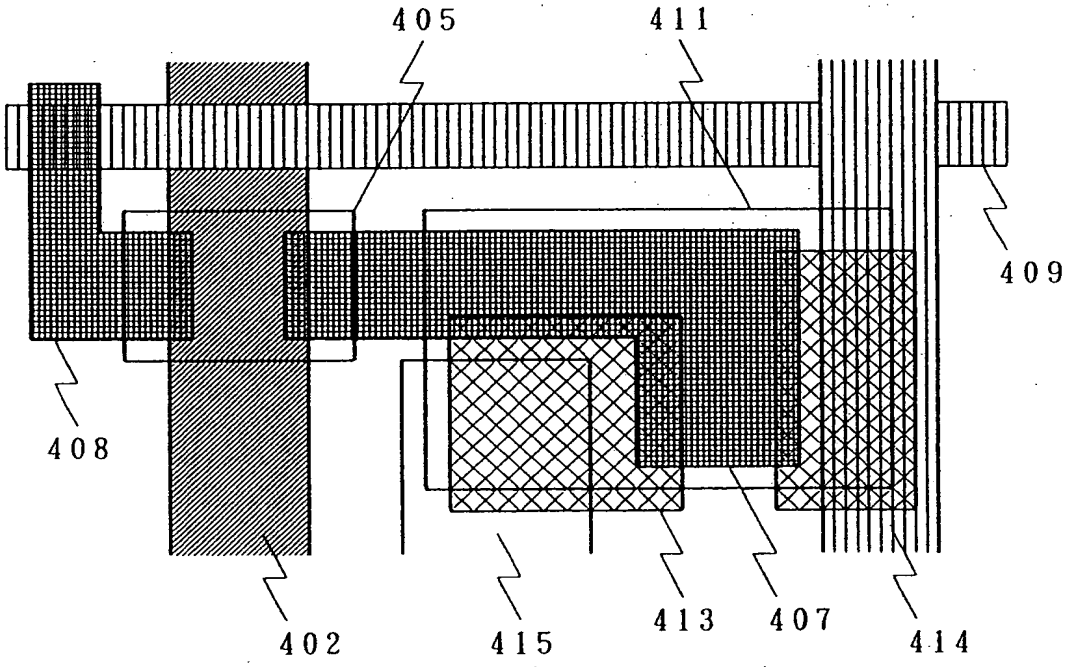

(B)